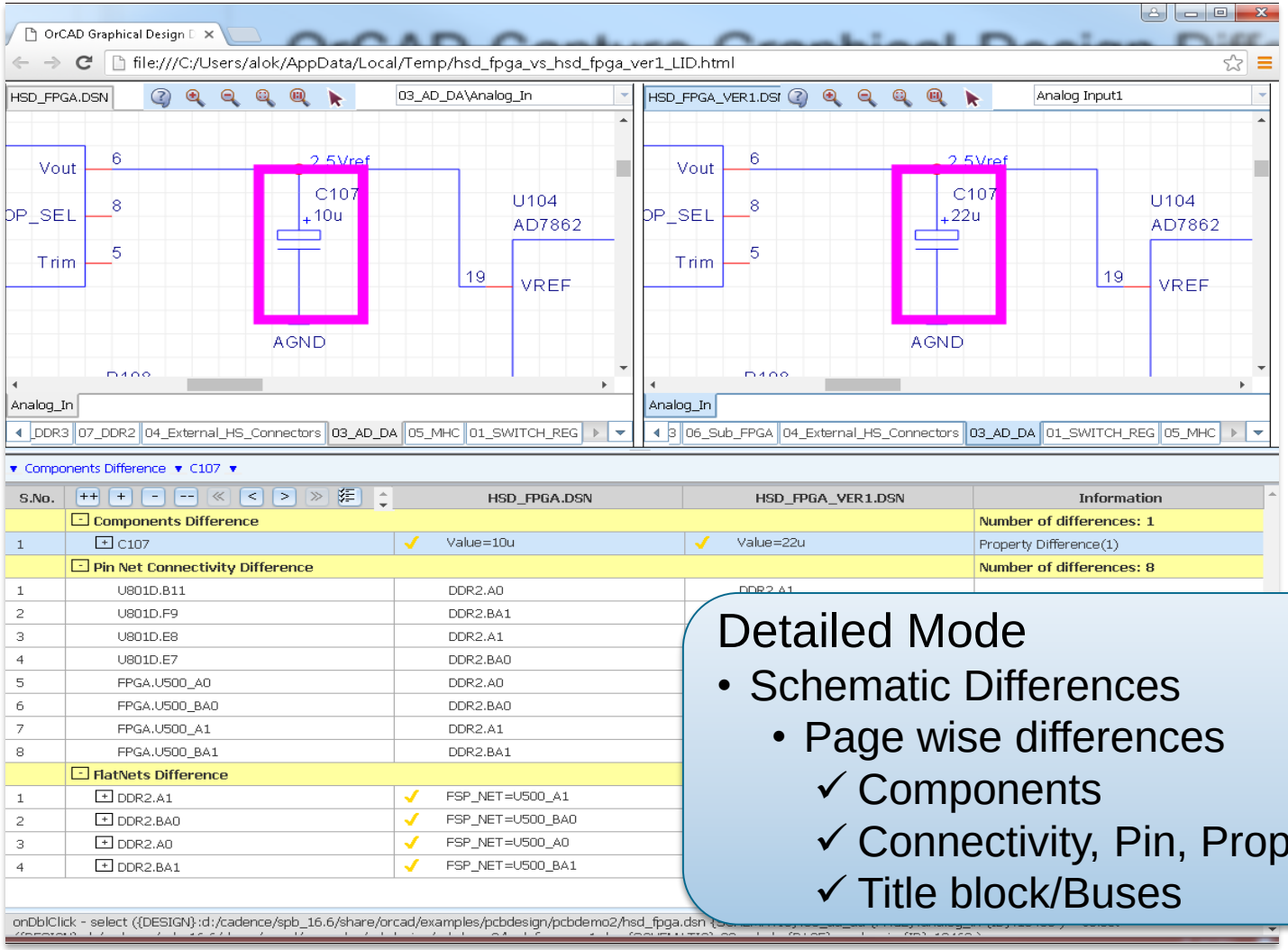
Agenda

- **Allegro/OrCAD релиз 17.2 QIR4 – QIR6**
  - Capture
  - PSpice
  - PCB Editor
- **OrCAD QIR 7 – планы на осень 2018**
  - Capture
  - PSpice
  - PCB Editor

OrCAD Capture – графическое сравнение схем

Визуализация отличий графически и в отчете



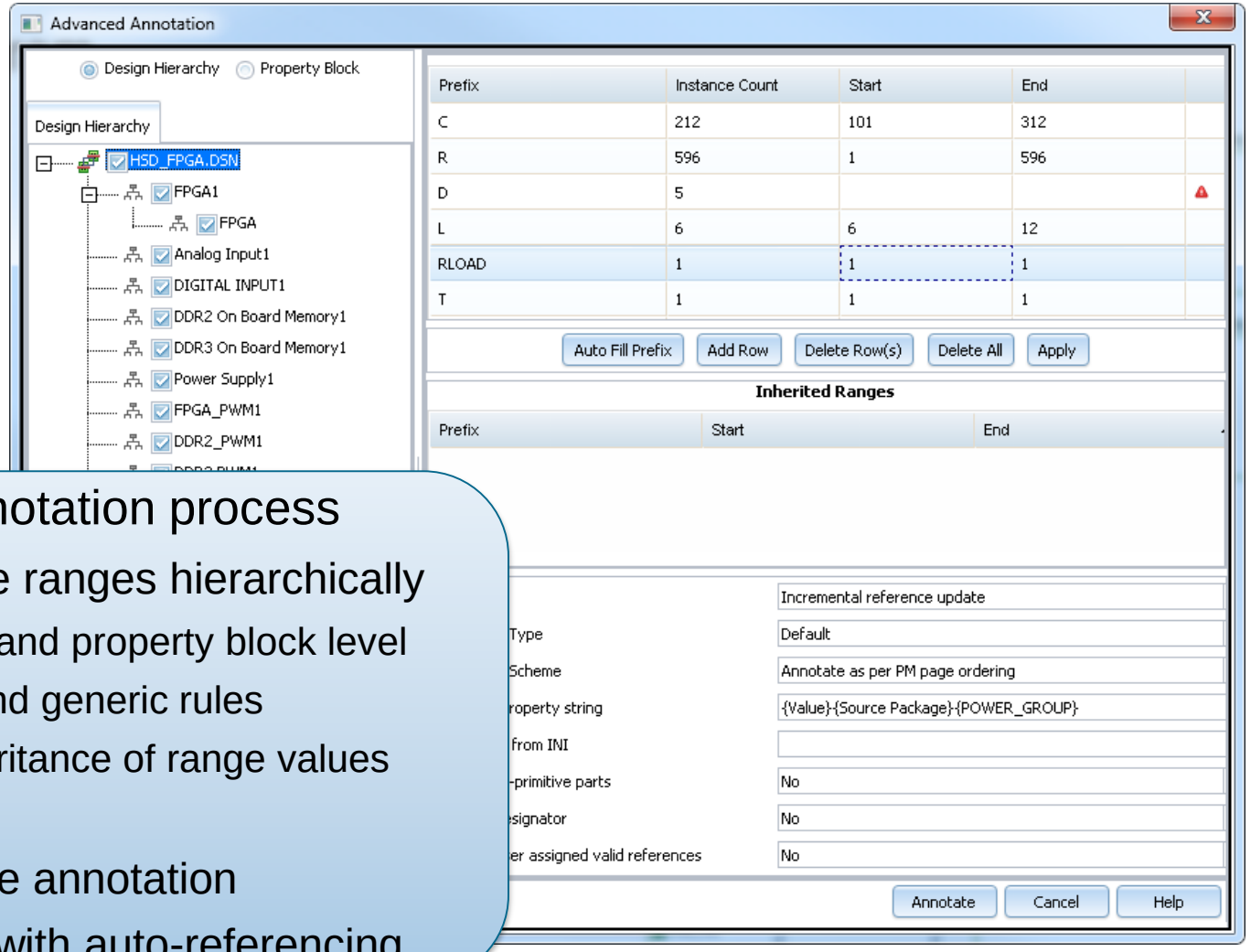
Detailed Mode

- Schematic Differences
  - Page wise differences
    - ✓ Components
    - ✓ Connectivity, Pin, Property
    - ✓ Title block/Buses

OrCAD CADENCE PCB SOLUTIONS

OrCAD Capture – продвинутая аннотация

Полный контроль над авто-нумерацией компонентов схемы



Control your annotation process

- Assign reference ranges hierarchically
  - At block, page and property block level
  - Prefix based and generic rules
  - Automatic inheritance of range values
  - Auto-scanning
- Perform selective annotation
- Fully integrated with auto-referencing

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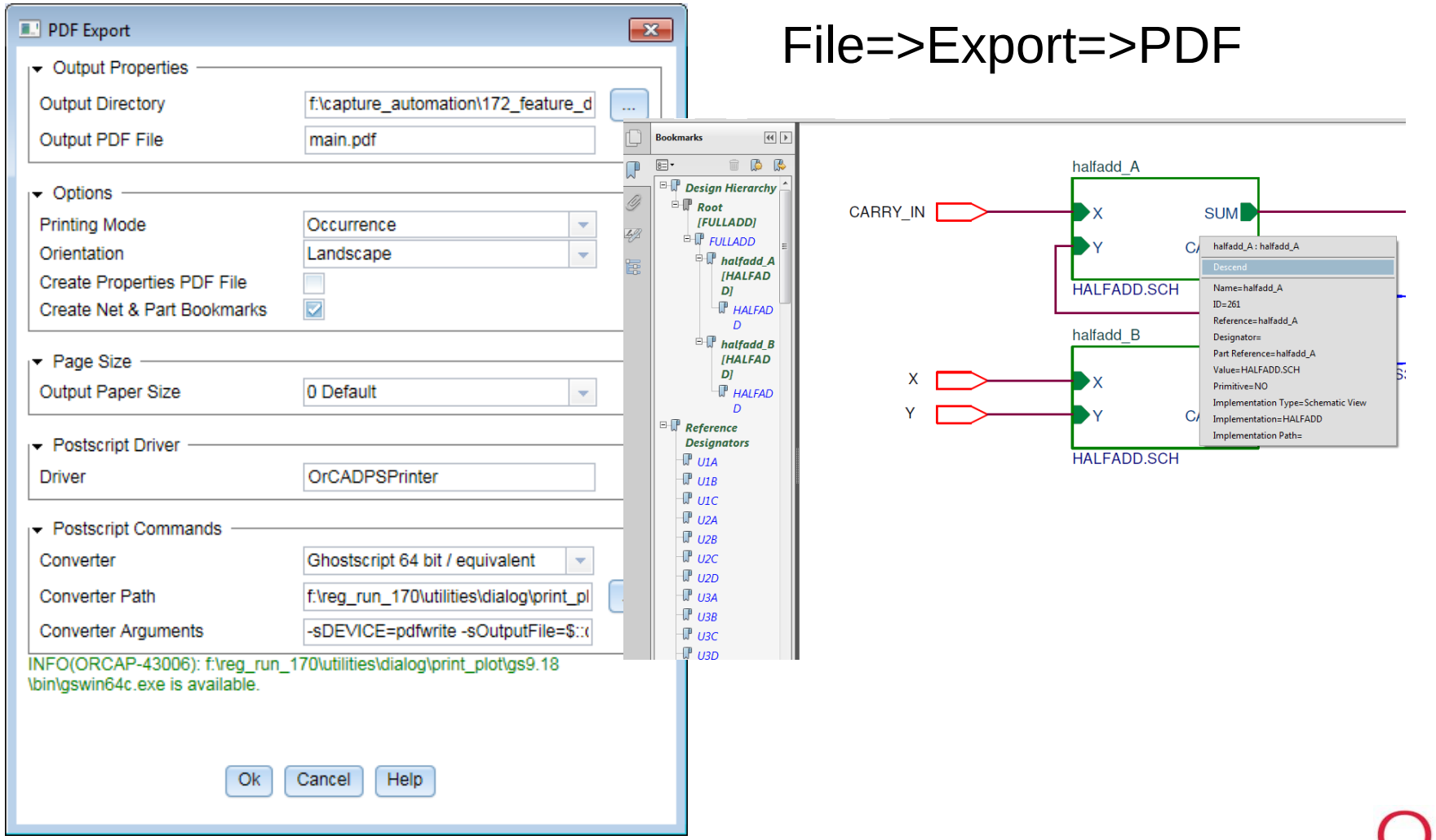
Экспорт PDF



File=>Export=>PDF

OrCAD
CADENCE PCB SOLUTIONS

Новый редактор УГО (символов на схеме)

- More anchor points on objects for precise draw
- Concise visibility of graphical objects and grid
- Integrated UI for modification increases productivity
- Unlimited number of UNDO and REDO
- Efficient selection of objects for intuitive drawing
- Define pin numbers for complete package in a single go
- Add or remove sections in package on the fly
- List of Supported pin / part properties defined in the UI itself
- Associate PSpice model while part creation
- Easily modify multiple pin for single section or all section

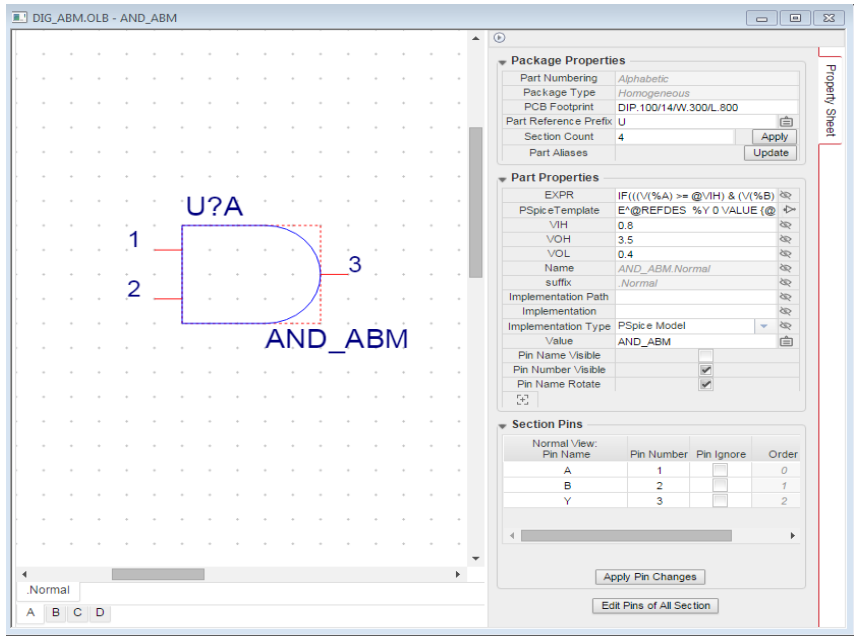
Key Takeaway

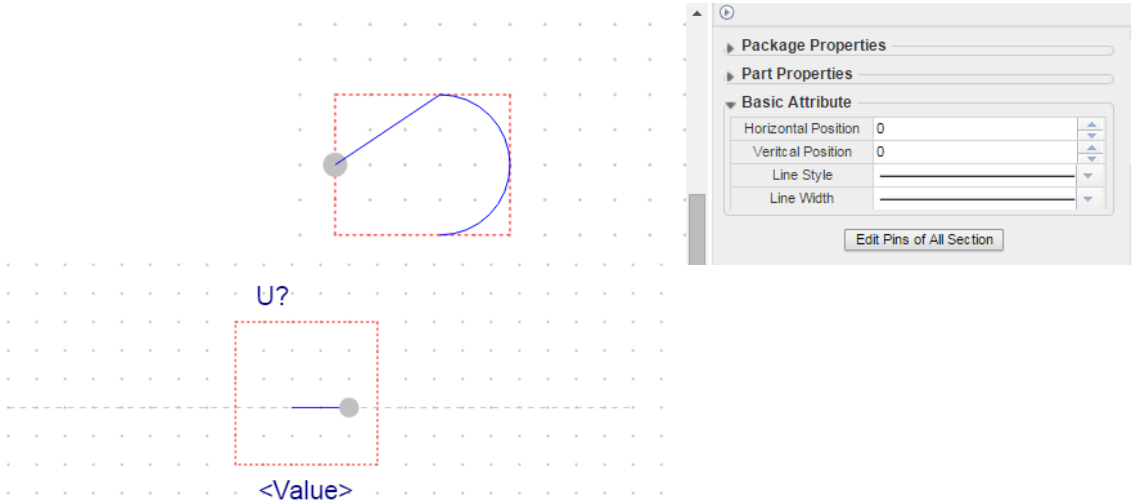
Enhanced Symbol Editor to help customers create new Symbols much quickly and easily

Новый редактор УГО

- New Single integrated UI
  - Single Click Access to :-
    - Part graphics
    - Package Properties
    - Part Properties
    - Pin Properties
    - Parts in Package
  - Configure FONT Style and Size

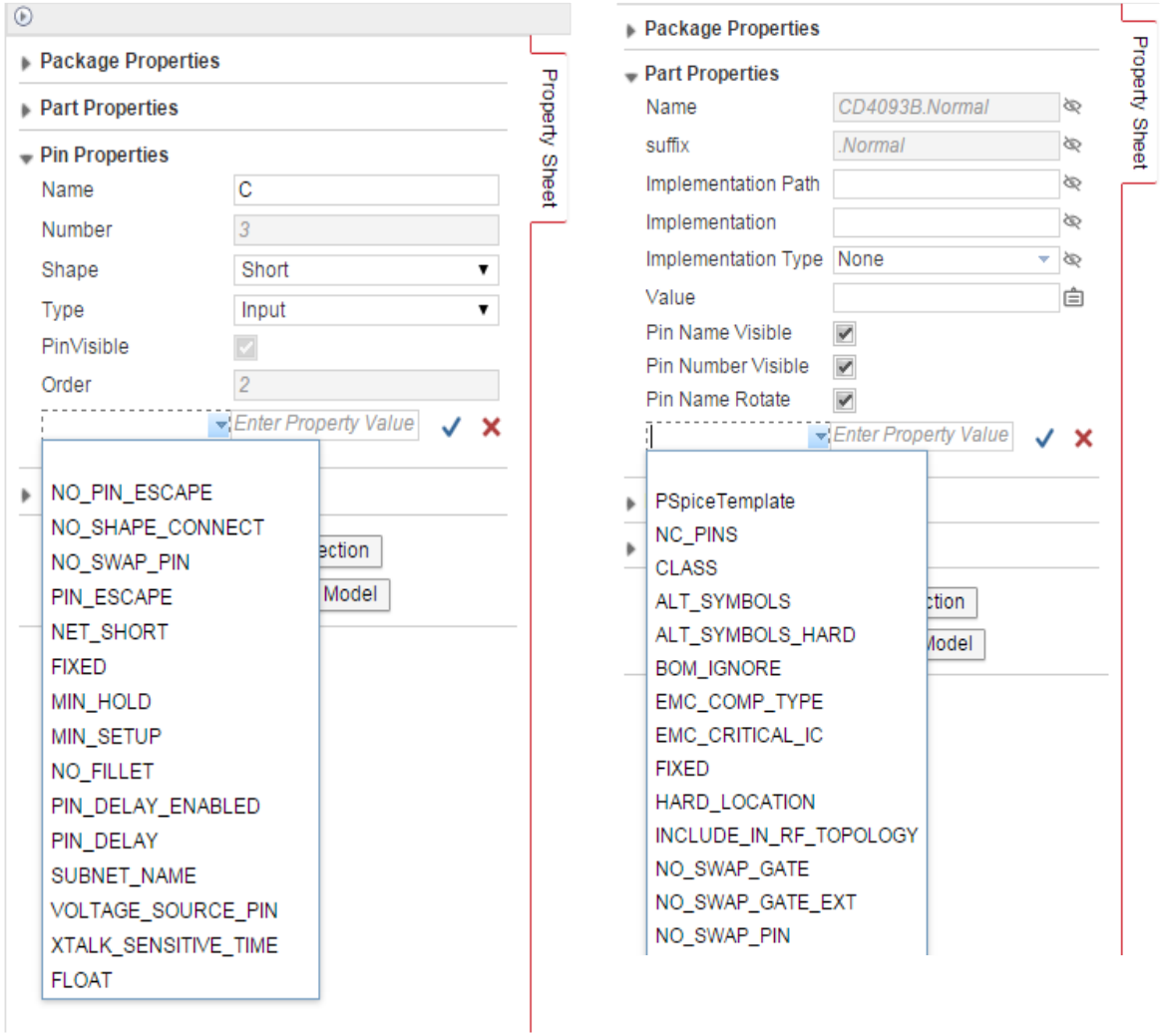
- Enhanced Productivity
  - Legible drawing
  - Unlimited UNDO/REDO
  - New Shortcut Keys
  - Smooth fine Grid movement
  - Positional attributes for objects
  - Efficient selection of overlapped objects





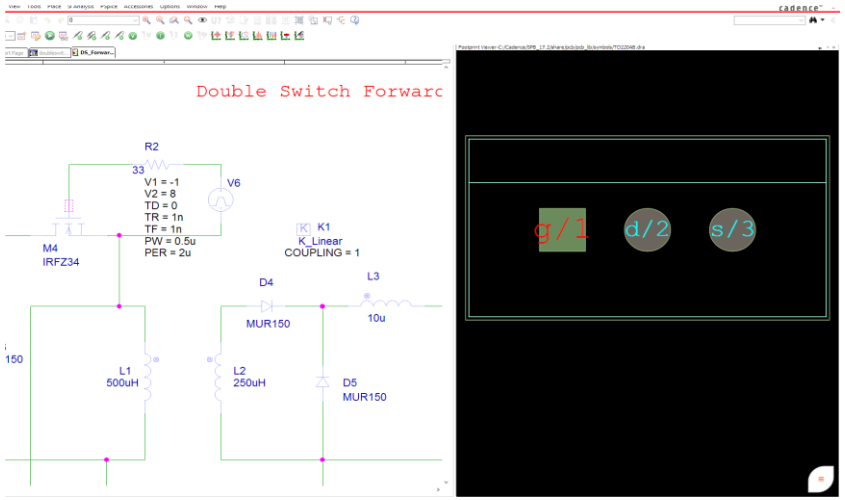
Удобная интеграция моделей PSpice

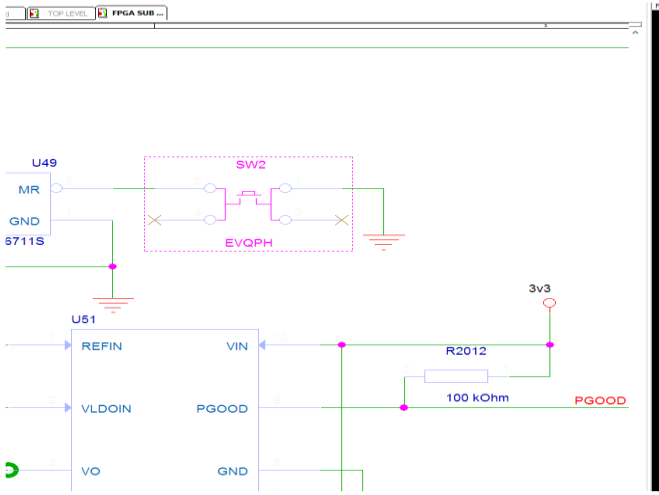
- New dropdown list
  - All supported part and pin properties while adding user defined properties
- Now associate PSpice model while creation

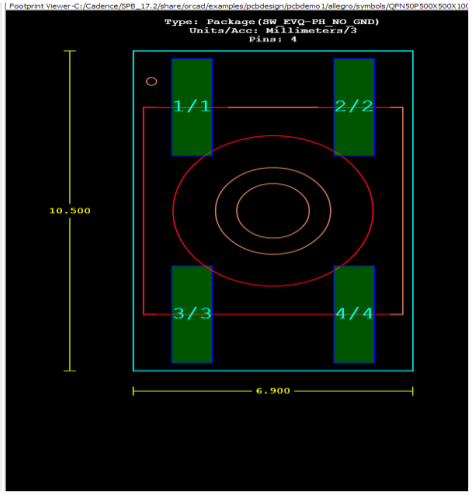


Просмотр футпринта в Capture

- Debug pin mapping
- Identify suitable footprint
- View footprint dimensions
- View footprint in schematic
- Cross-probe viewer / schematic
- Turn on / off pin name / number
- See additional footprint details

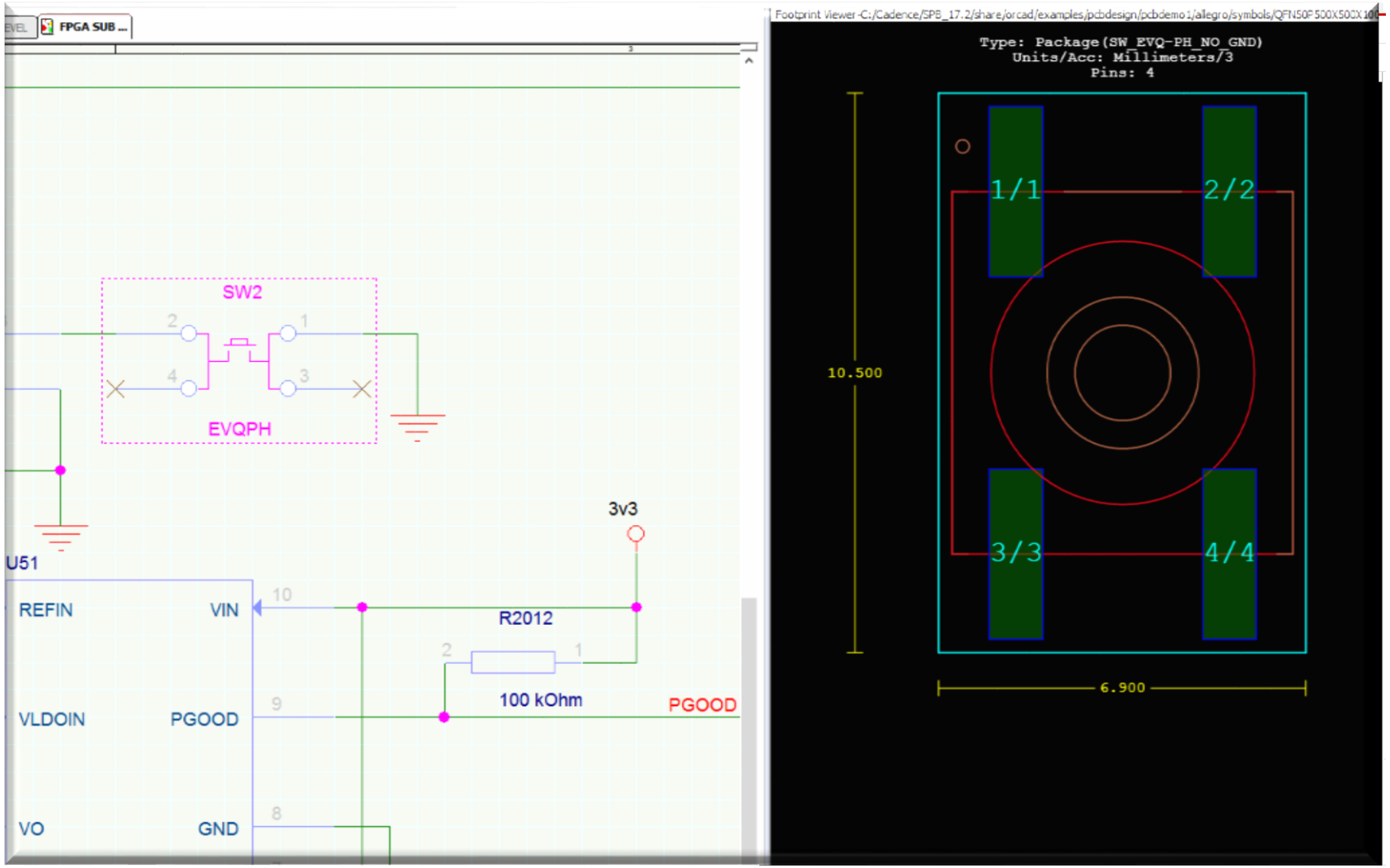






Просмотр футпринта в Capture

- Ability to view footprint from schematic instance
- Ability to cross-probe between viewer and schematic
- Ability of turn on/off pin name/number in viewer
- Ability to see additional details about footprint
- Available for all Capture licenses



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PCB Editor QIR4 – QIR6

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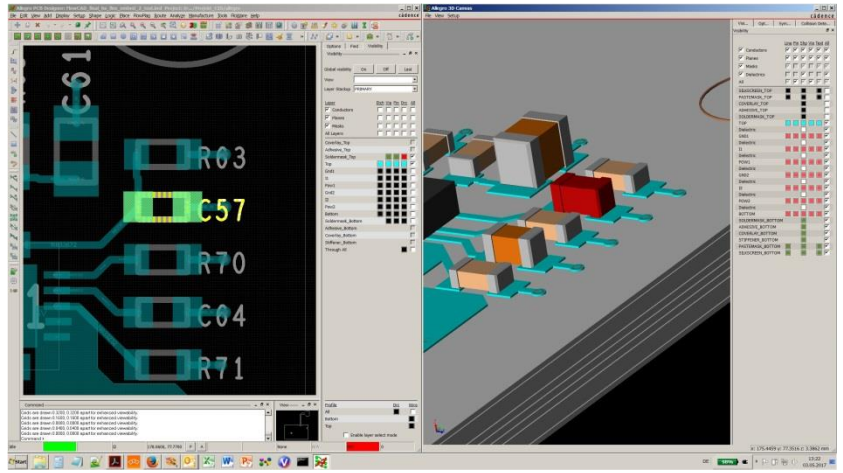
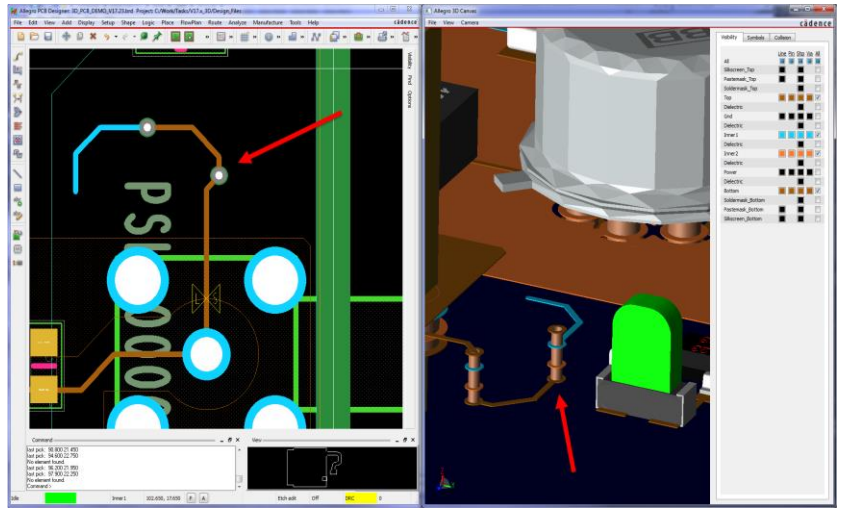
Новый 3D-редактор

- 3D Enhancements in 2017 have been Significant!
- We have actually caught up on 3D
- We are working on improving the overall 3D Bring-up Performance
- Customers using the solution in production designs
  - Cross probing between 2D and 3D
  - Design updates in 2D are immediately visible in 3D Canvas
  - Collision Detection
  - Zone Aware 3D
  - Clearance check
  - Etch layers visibility control
  - Measurements
  - …..



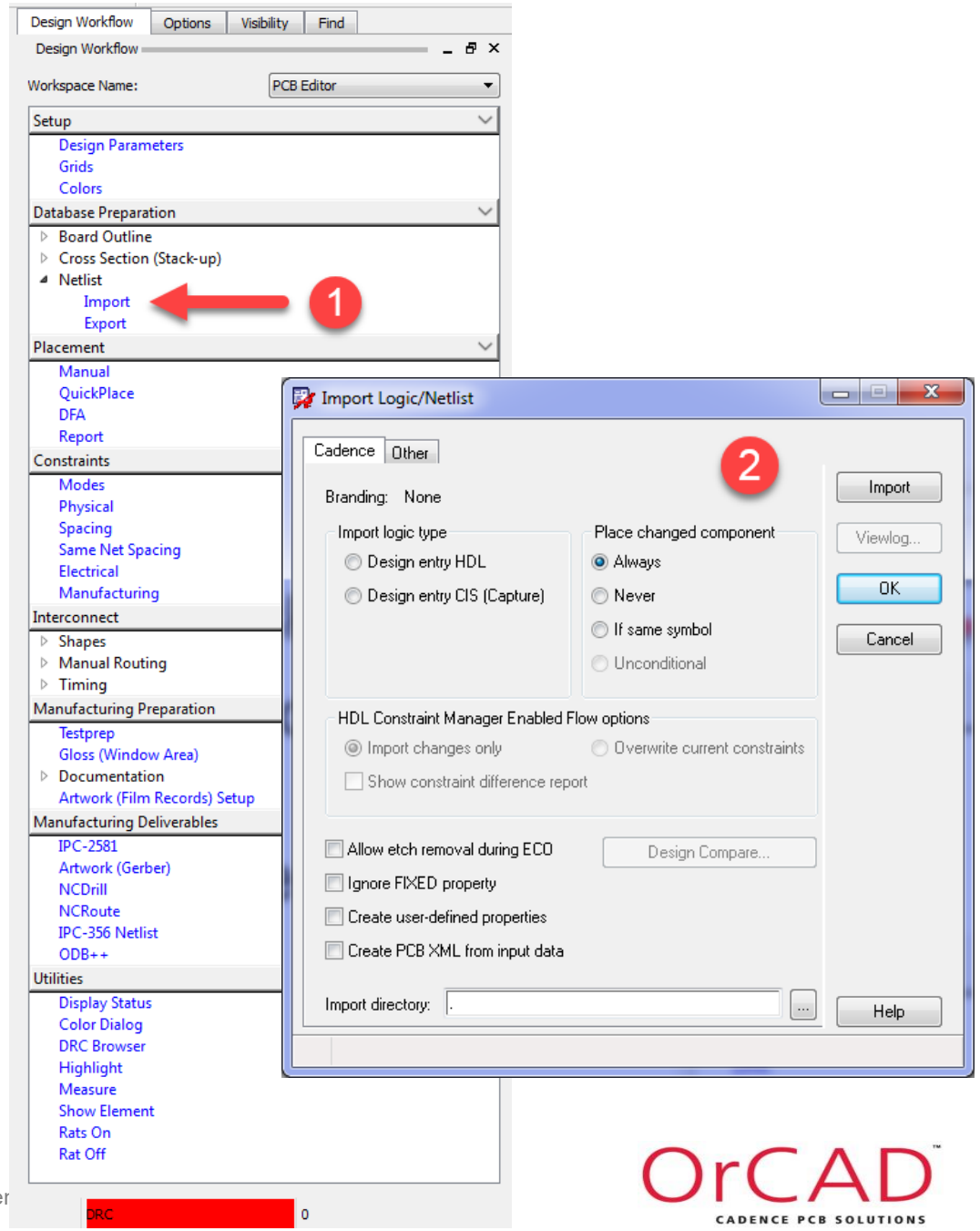


Allegro PCB Editor Improvements in 2018

- New Allegro Canvas
  - Start page
- Productized Interactive 3D Canvas
- Allegro PCB DesignTrue DFM
  - DFF in QIR4
  - DFA in QIR6
  - DFT in QIR7
- Sigrity Technology Driven High Speed Analysis and Checking
  - Impedance analysis and vision
  - Coupling analysis and vision
- Symphony Team Design
- Sneak Peek at QIR7

Панель «маршрут проектирования»

- Guide users in performing basic tasks
  - Good for new and experienced users
  - Leverage experienced designers good practices for junior / new users
- Eliminates search icons or menus
- Selecting any choice will bring up proper dialog
- Create custom flows
  - Examples such as library creation, internal checklist, manufacturing deliverables
    - XML file format

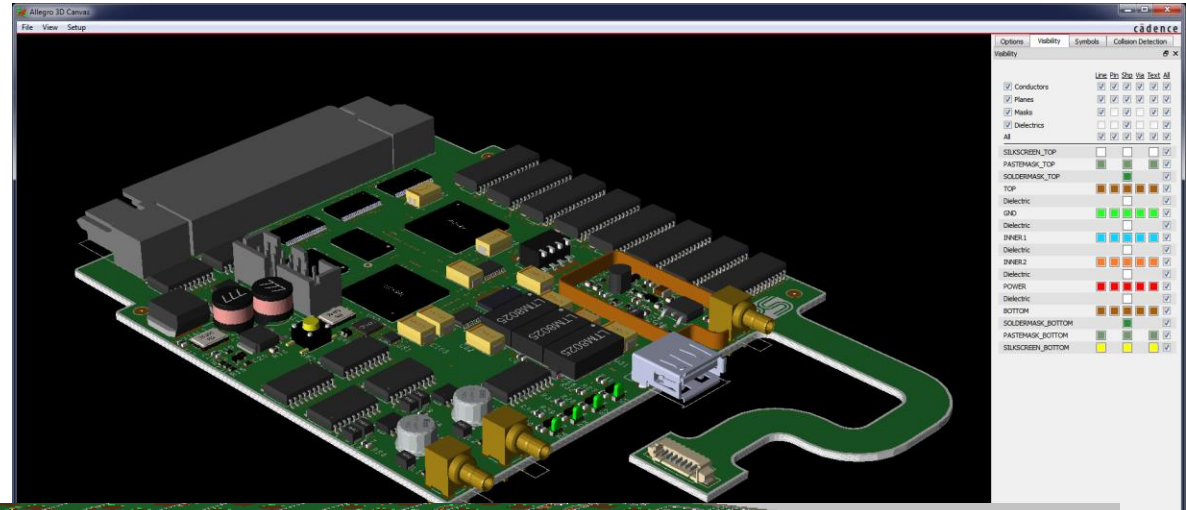


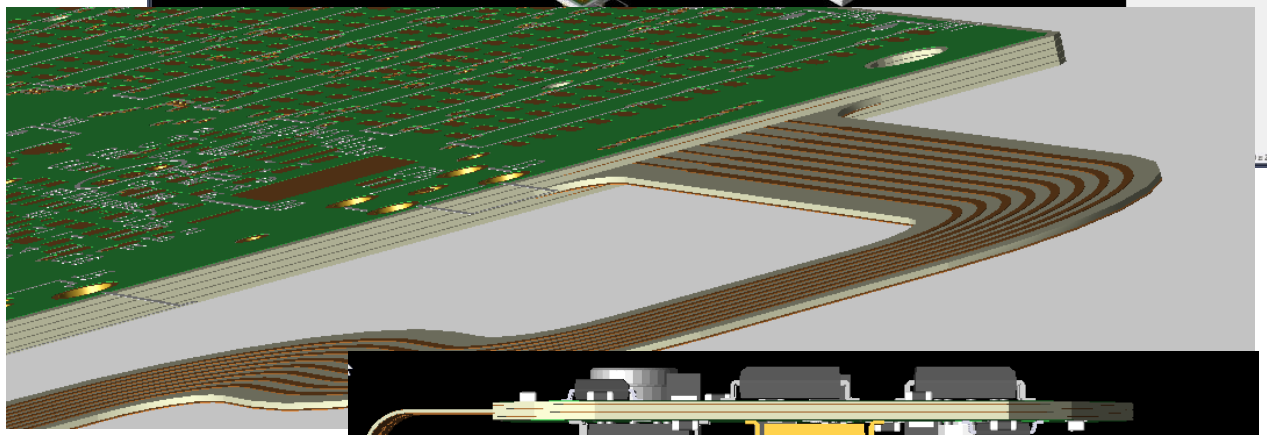
Улучшенный интерфейс пользователя

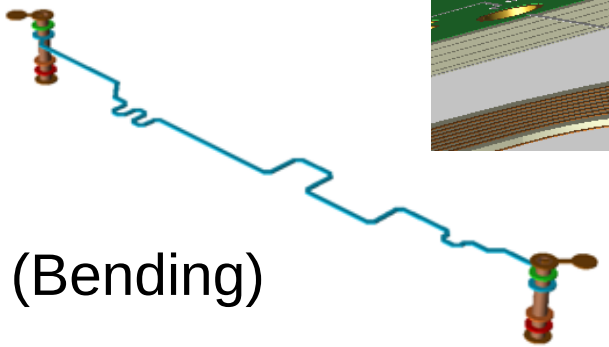
- Minimalistic Toolbars and Icons
  - Reduces clutter and confusion
  - Presents new users with only relevant icons
  - Full toolbars and icons available
  - Increased design work space
- Customize Design Canvas
  - Toolbars, Panes and Workspace
  - Save/recall views
  - Includes panes on other monitors
  - Manage from the View – UI Settings menu

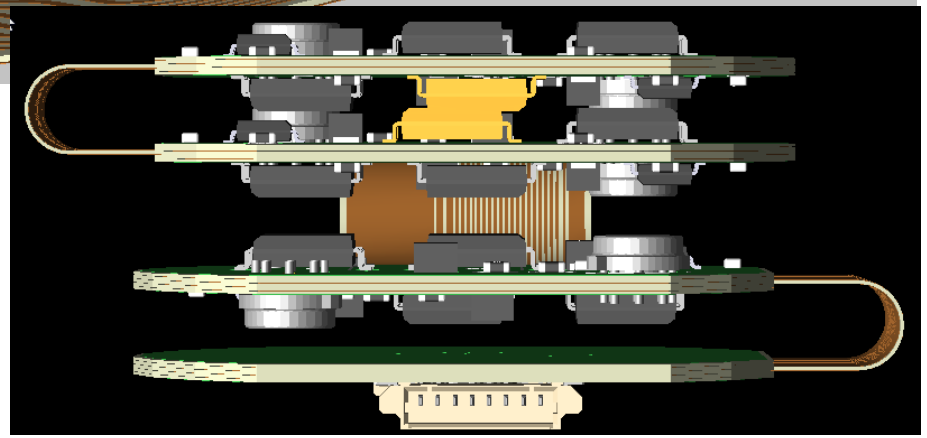
Мощный 3D-редактор

- Completely NEW 3D Graphics Engine
- 3D to 2D Communication i.e. Real Time Updates
  - Cross Probe, Highlight, Edit, Move, Undo/Redo
- Full Layer Modeling and Visibility
  - Etch - Mask – Silkscreen – Lines - Pins
  - Vias - Dielectric – Paste – Text - Shapes
- Symbol Visibility Controls
- Collision Detection
- Zone/Stackup Aware
- Export Capabilities
  - HSF, HMF, OBJ, PLY, STL
- Rigid-Flex Transformation (Bending)
- Support for Cover Lay









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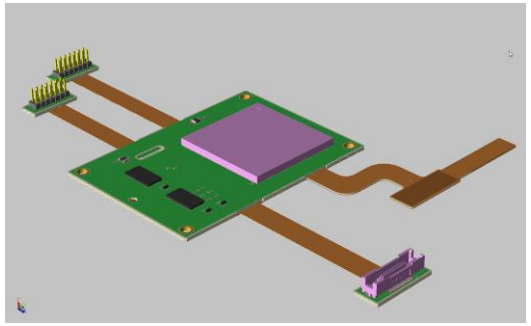
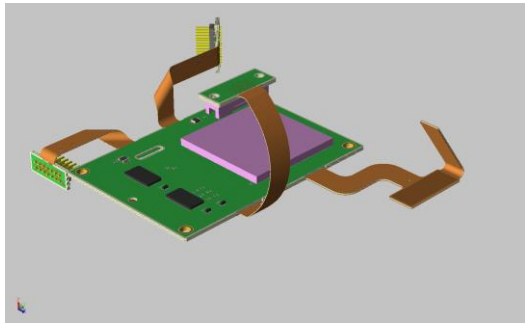
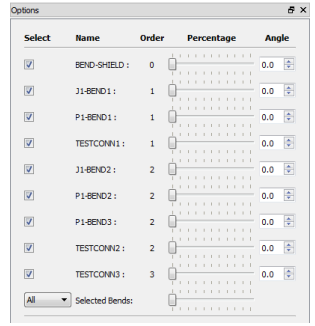
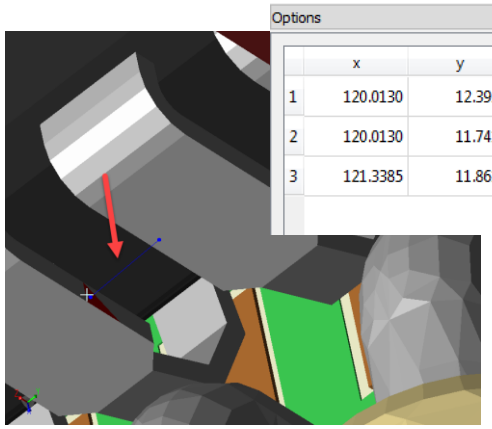
Улучшения в Allegro 3D

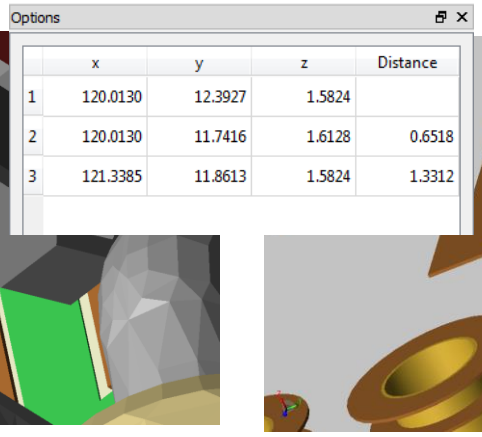
- Rigid-Flex Transformation (Bending)
  - One slider for each bend + an ALL slider
- Measure Path between two or more points
  - Accumulative
  - Measure between STEP model surface or 2D design elements
- Cross Section Views
  - Sliders allow views at any point of the design
  - X, Y & Z Alignment
  - Tilt in any axis

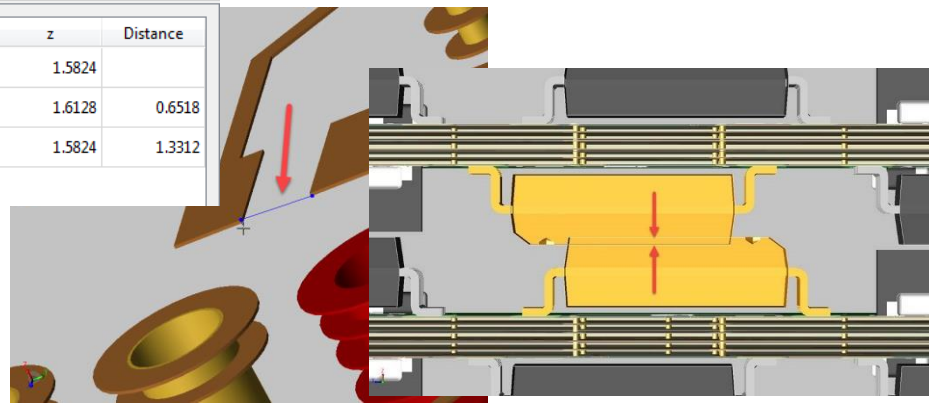


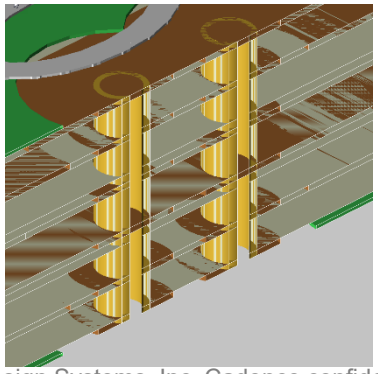


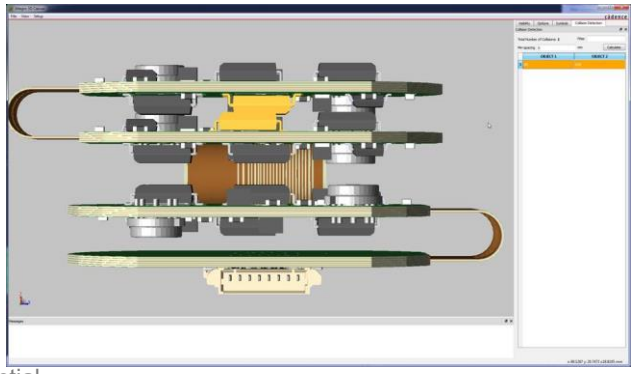












Allegro PCB DesignTrue DFM
Анализ технологичности проекта с точки зрения производства

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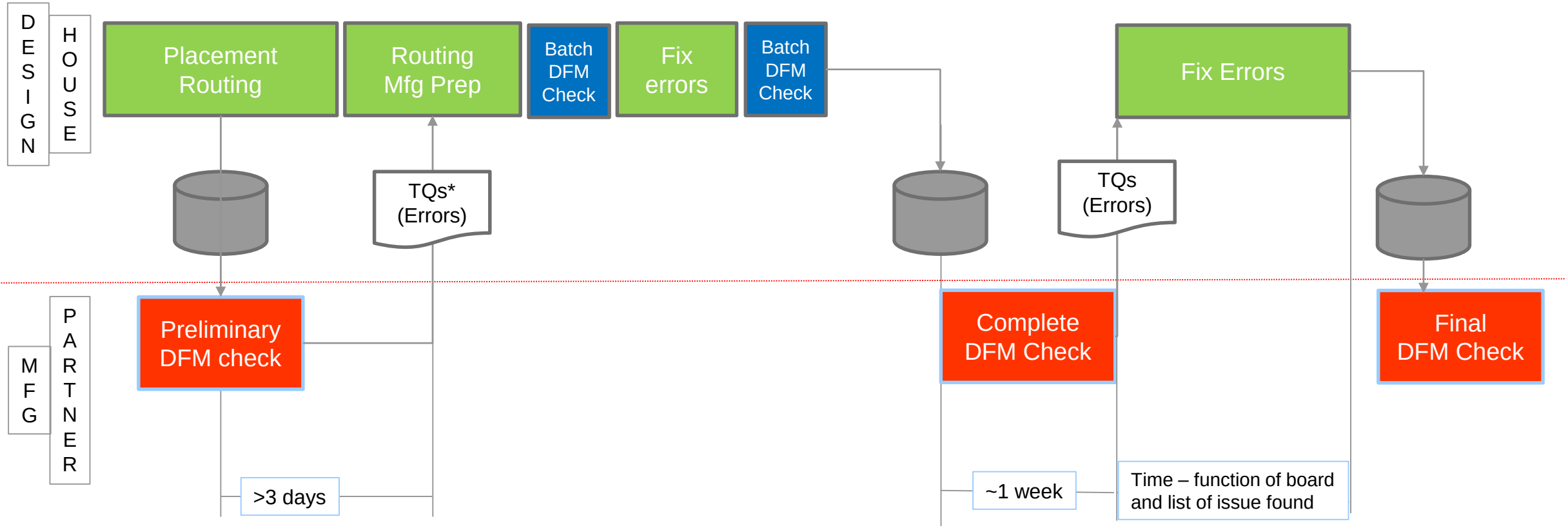
Обычный маршрут с DFM-проверками после разработки

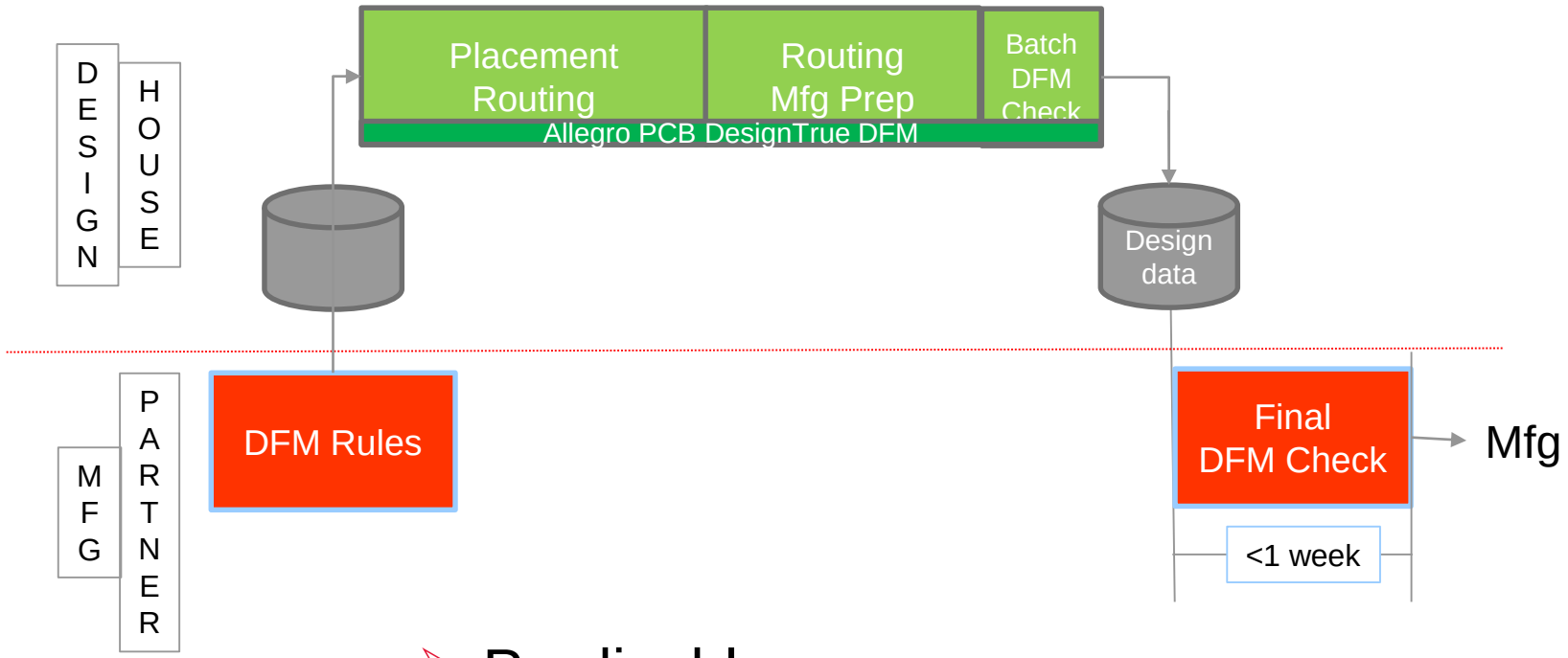
- Unnecessary iterations with the manufacturing partners
- Lots of pressure because it is the LAST step before the product can be built / shipped



*: TQs: Technical Queries

Ускоренный маршрут с Allegro PCB DesignTrue DFM

Manufacturing rules-driven design



- Allegro® PCB DesignTrue DFM provides
  - DFF and DFA rules
  - Over 2000 advanced checks independent of electrical rules
- Real-time checks as you design
  - Signoff with confidence
  - Save at least one day per iteration
- Ensures design is ready for manufacturing
  - While shortening the development cycle
- Easy to use, reuse, and apply selectively, exclusively, or globally

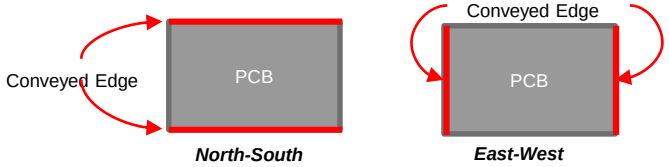
- Predicable process
- Much shorter design cycle
- Faster product introduction

* Over 200+ Core checks in Allegro PCB Designer
Over 2000 Advanced checks in **Allegro Venture PCB Designer**

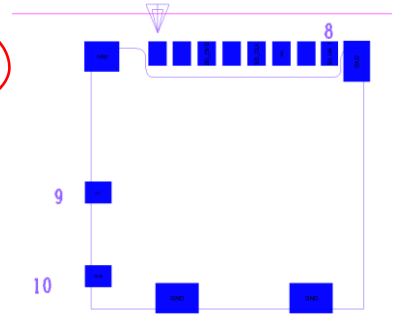
Проверки Design for Assembly (DFA) (QIR6)
Extensive checks for assembly process

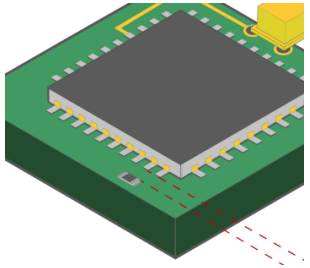
- Outline checks
  - Component to board outline*
  - Tall component conveyed edge (board outline)
  - High pin-count component to board outline
- Component checks
  - Component pin to component body*
  - Edge finger to component body
  - Mechanical hole to component body*
  - Via under a small outline component
  - Trace under a small outline component
- Fiducial checks
  - Fiducial to component body
  - Number of fiducials per footprint
  - Inside/outside body location checks
- Pastemask checks*
  - Pastemask to outline / cutout check
  - Pastemask to pastemask check
  - Pastemask to via pad check
  - Pastemask size to SMD pad size
  - Missing pastemask for SMD pins
  - Pastemask to soldermask pad ratio
  - Pastemask to coverlay pad ratio

Conveyed Edge
North-South or East-West

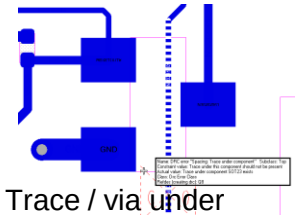


Component to board outline

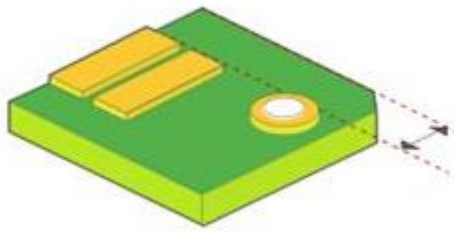




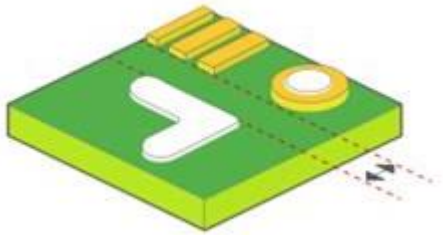
Component pin to component body



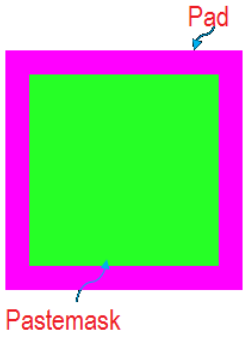
Trace / via under a small outline component



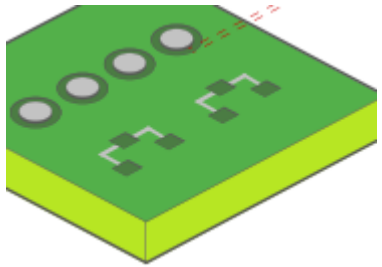
Pastemask to Board Outline



Pastemask to cutout



Pastemask to SMD Pad size



Pastemask to soldermask or coverlay pad ratio

***: Core checks**
All other checks: advanced checks

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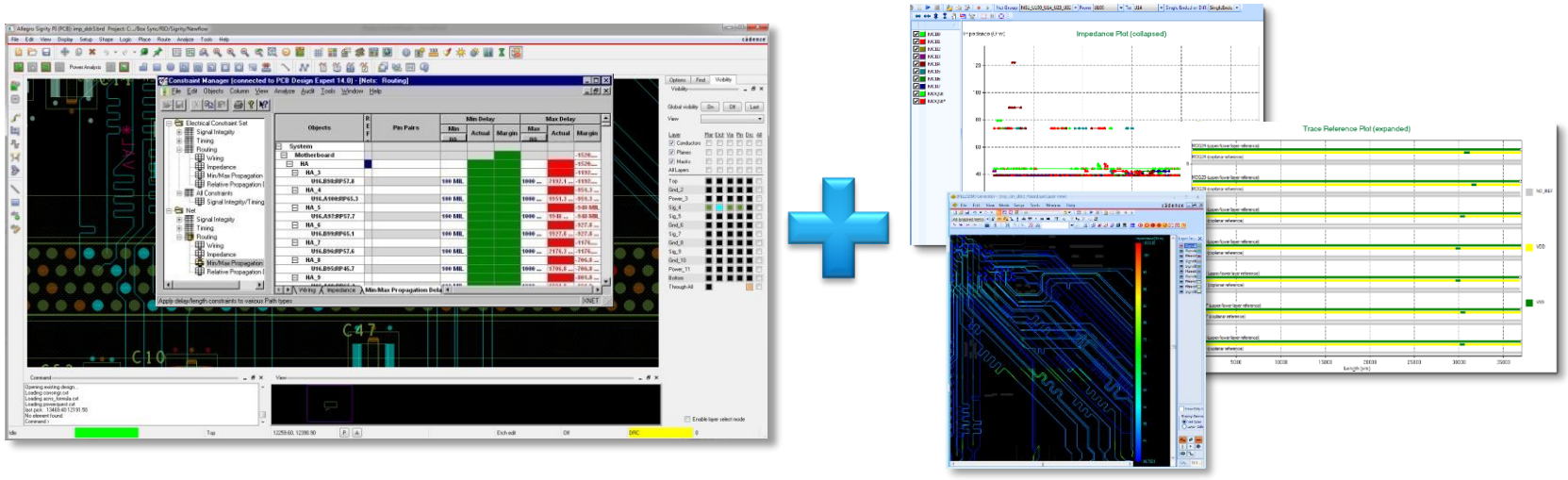
Стыковка с маршрутом анализа скоростных сигналов Sigrity

OrCAD™
CADENCE PCB SOLUTIONS

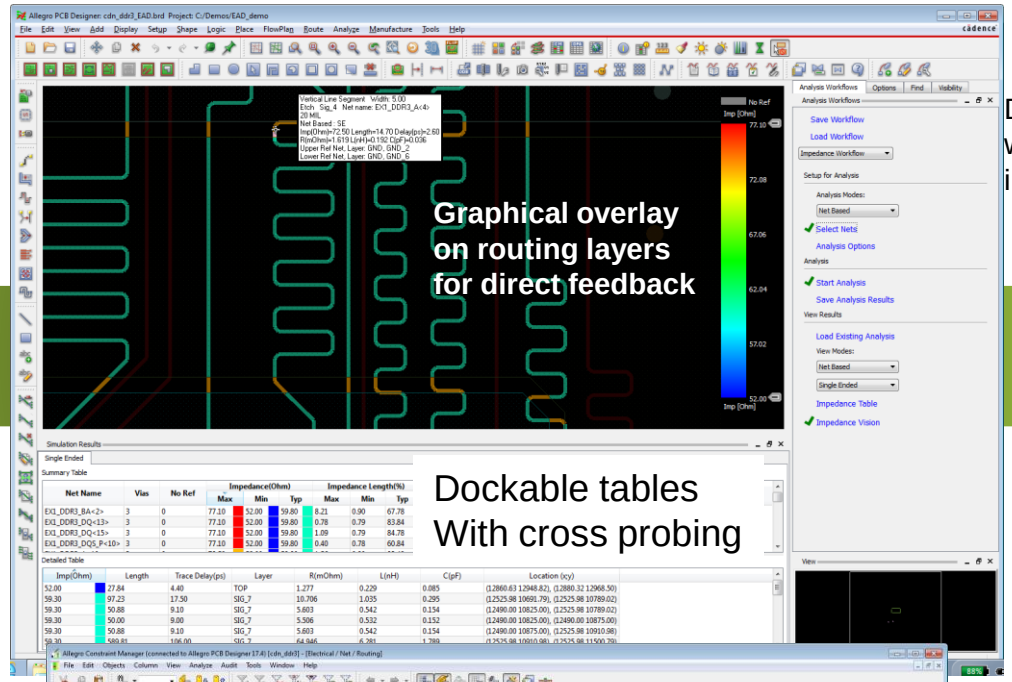
Анализ Sigrity внутри Allegro QIR4

- Constraint Manager as single cockpit for all rule checking
- New analysis flows with enhanced results viewing
- New rules and overhaul of existing to significantly increase DRC / ERC / coverage
- Powered by Sigrity Technology



Sigrity Analysis within Allegro environment
Two flows – Analysis and Checking – QIR4

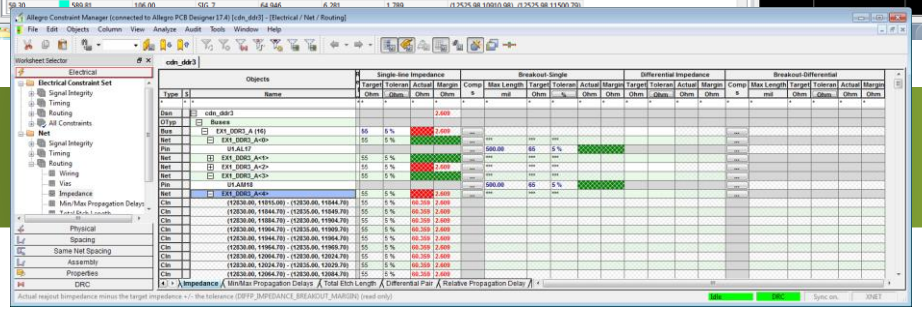
Analysis Flow



Dockable Sigrity workflows natively in Allegro PCB Editor

Analysis results on canvas

Checking Flow



New DRCs and existing worksheet overhaul in Constraint Manager

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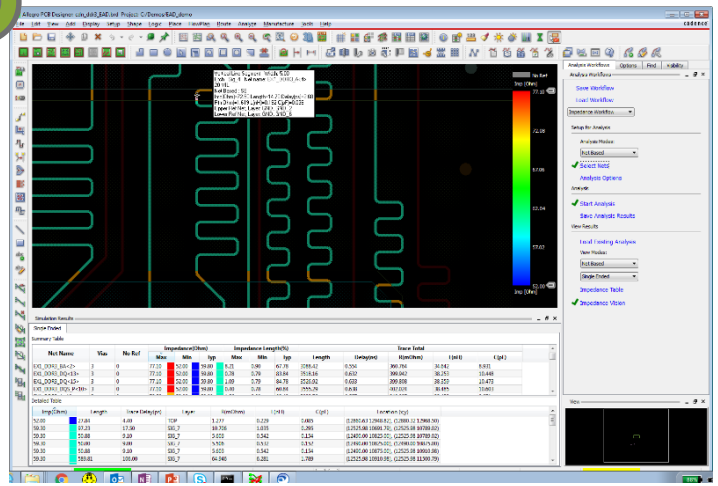
Контроль трассировки с точки зрения целостности сигнала (Allegro PCB High Speed Option)

- Available in QIR4
- Eliminate unnecessary iterations with SI/PI engineers
- All three supported in Symphony Team Design Option

1 Impedance Analysis and Vision



Analysis data on canvas and in tables
Cross-probe, zoom into problem areas

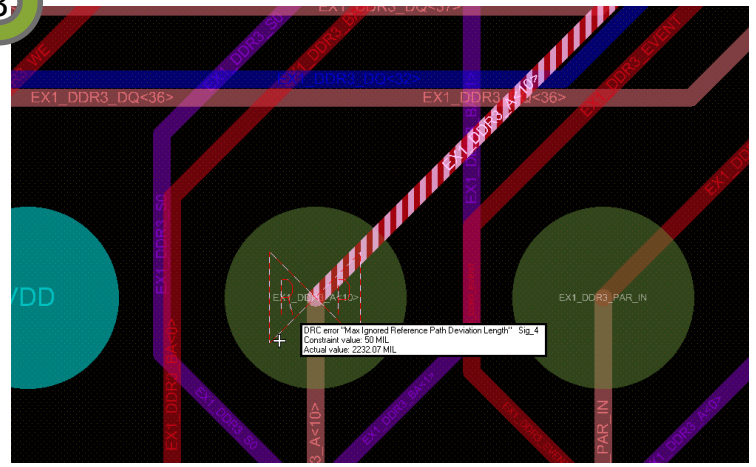
Quickly identify nets that are out of spec
Sliders on scale allow for filtering of view

2 Coupling Analysis and Vision

View victim and aggressor
nets on canvas

Quickly identify nets that are coupled
Sliders on scale allow for filtering of view

3 Return Path DRC



Signal not next to
required Ground Plane

Identify critical nets without a
reference plane quickly
Above or below or both

Параллельная трассировка Symphony Team Design

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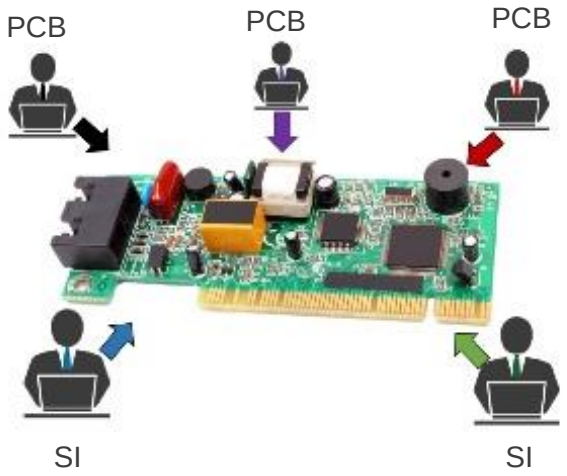
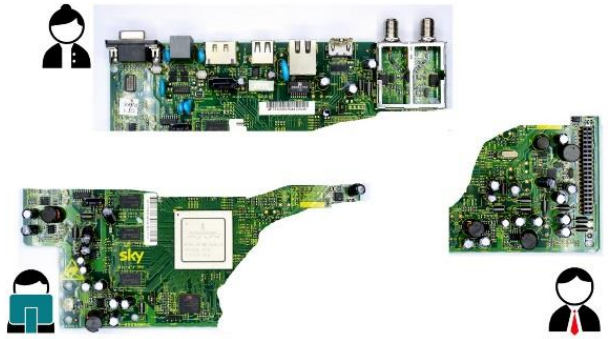
Allegro PCB Team Design Options
Two ways to leverage the power of your team

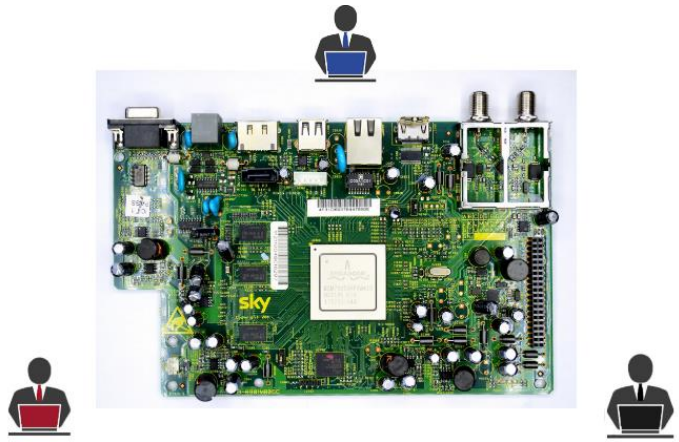
Concurrent Design
with shared canvas

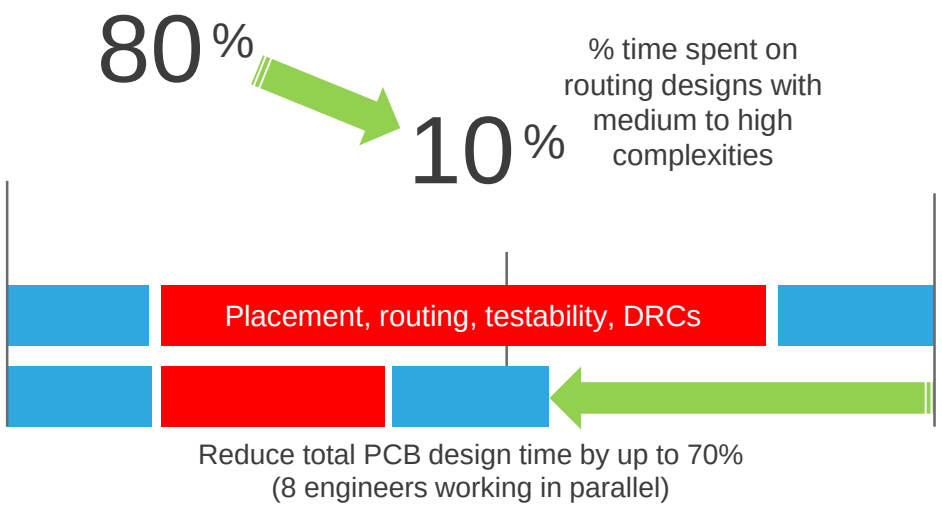


Distributed Design
with partitioned canvas



Allegro PCB Symphony Team Design Option
Concurrent design with shared canvas





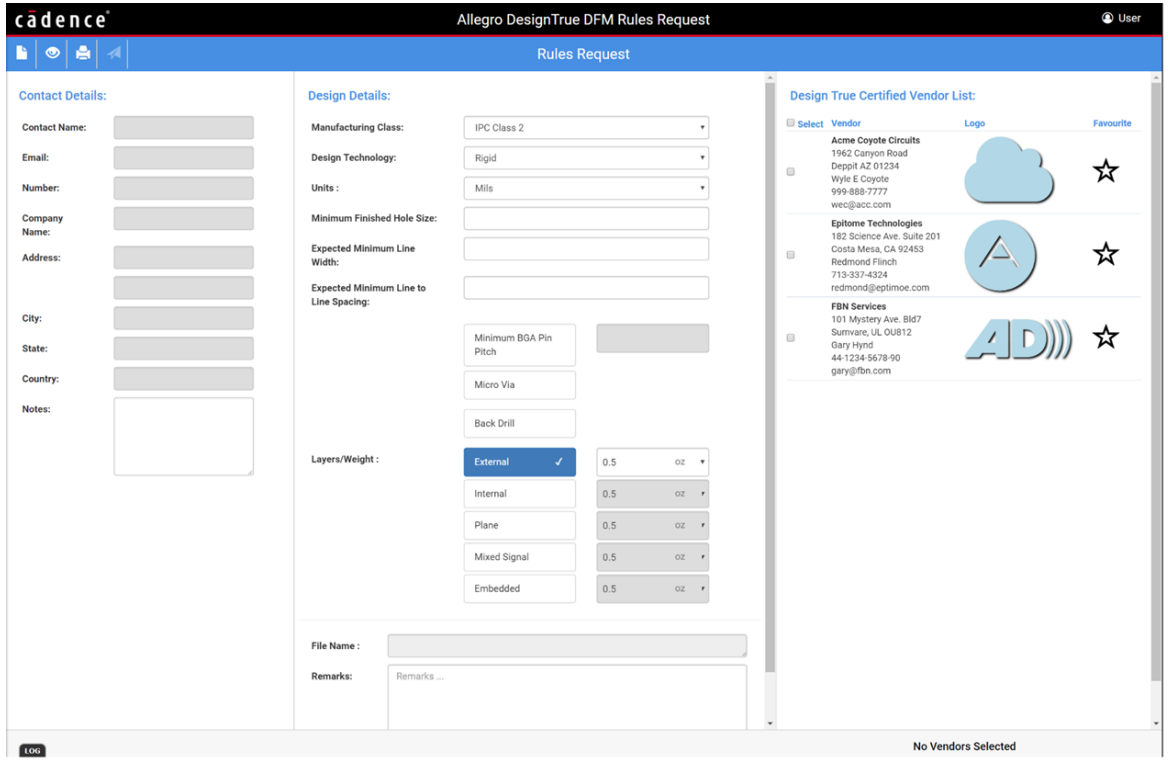
- Multiple PCB designers access a common PCB layout database
- Everyone co-designs together in real time
- Easy setup eliminates copy/paste database “chaos”

Новые возможности в осеннем QIR7 Allegro PCB Editor

OrCAD™
CADENCE PCB SOLUTIONS

DesignTrue DFM – поддержка тестовых точек

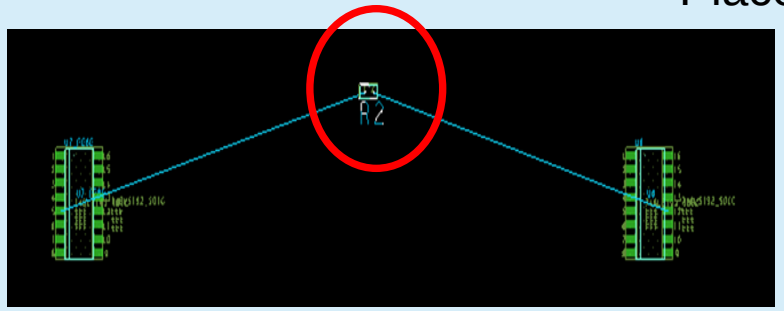
- DFF support introduced in QIR4, DFA in QIR6
  - QIR7: Lead to Pad check
- Design For Test (DFT) support in QIR7
  - Test points to other objects checks
  - Test point size and location checks
- DesignTrue DFM web portal for customers to get access to manufacturers that provide rules in Allegro format
  - Define technology needs
  - Find manufacturers that support your needs and provide rules in Allegro format



OrCAD CADENCE PCB SOLUTIONS

Улучшение процедуры размещения компонентов Placement Vision (QIR7)

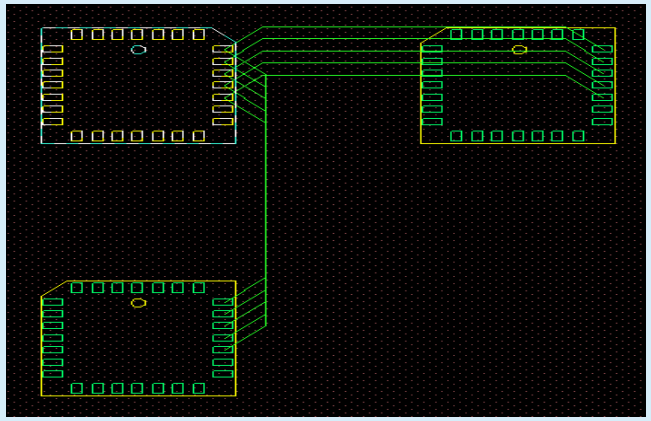
Placement Vision: Xnets



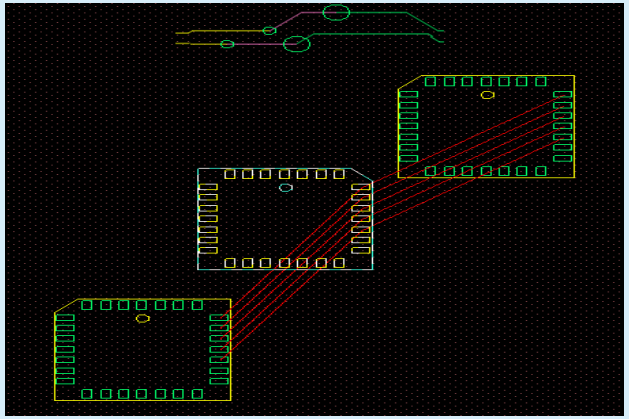
Normal ratsnest display

Ignores connections to series inline resistors/capacitors to show the signal path

Placement Vision: Ratsnest timing



Passes max length displayed in green

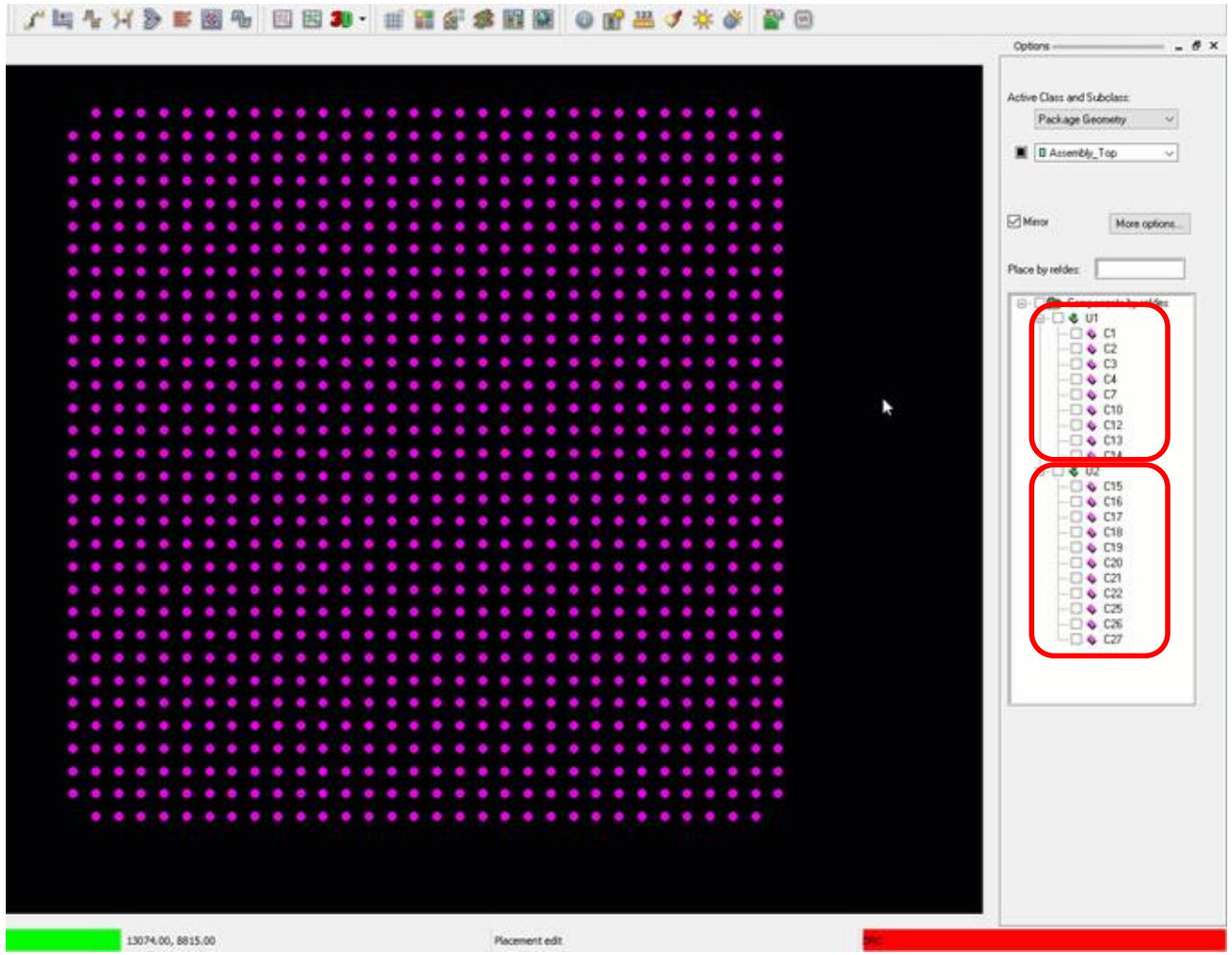


Fails max length displayed in red

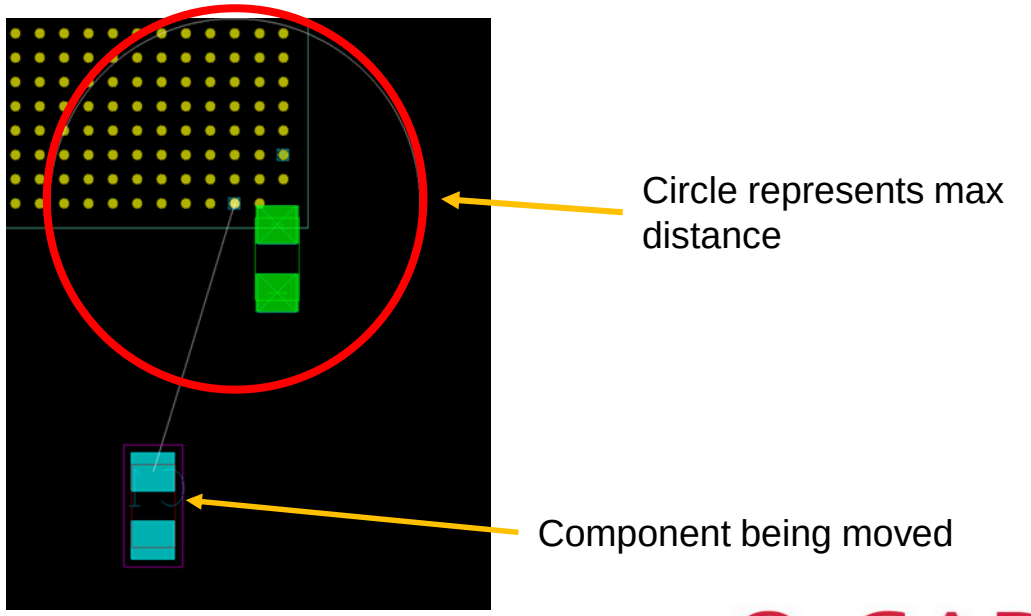
- Min/Max Prop delay
- Total Etch length
- Calculations based on manhattan distance
- Rat colors update dynamically

OrCAD™ CADENCE PCB SOLUTIONS

Контроль расстояний от микросхемы до блок.конденсаторов

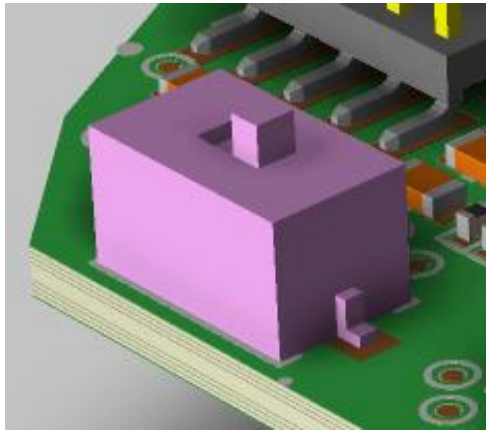


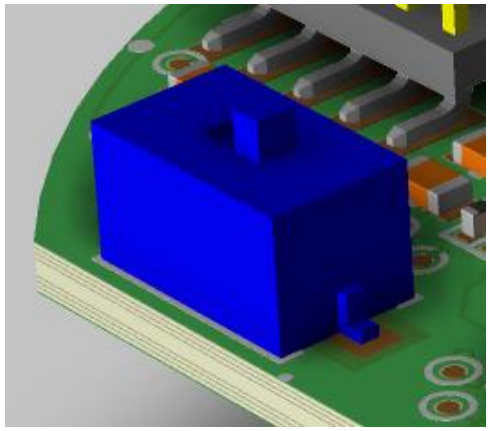
- Associate decoupling capacitors to an IC pin in Allegro SDA with max distance
  - Associations passed to Allegro PCB Editor including max distance to parent pin
- Quickplace places all associated components to the parent pin location (Top or Bottom side)



3D-редактор QIR7

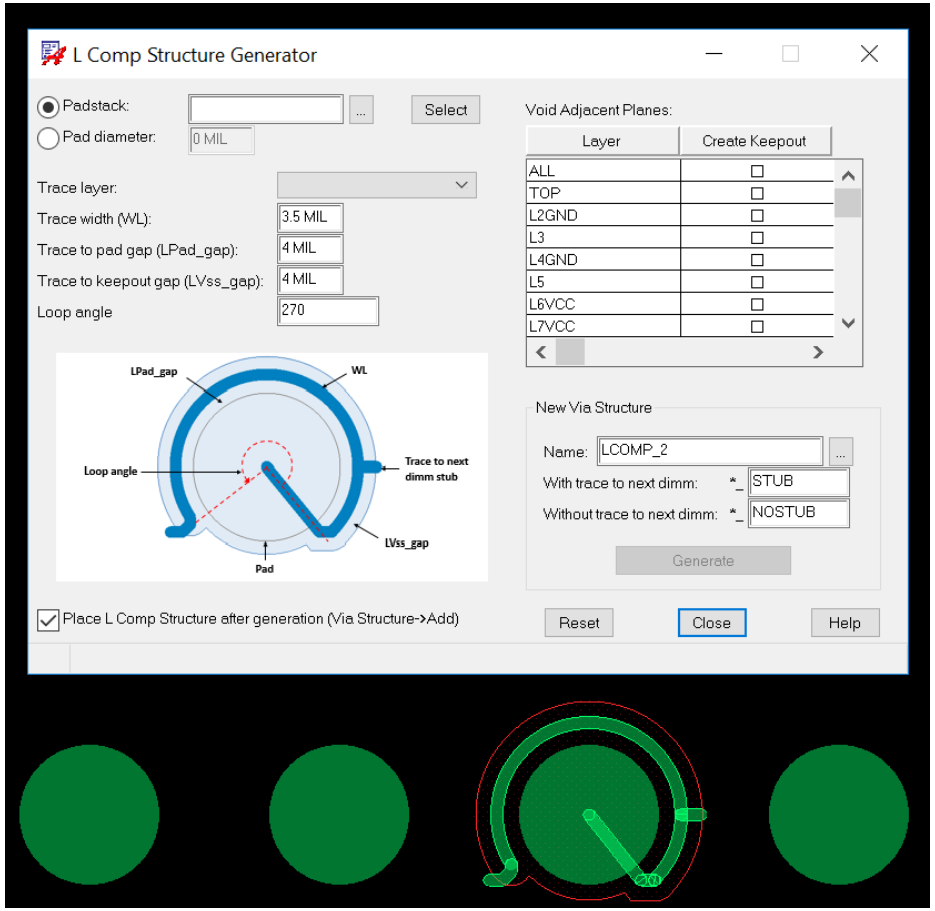
- Layer Transparency
  - 8 color themes
  - Added sliders for different layers
- Cutting Plane Reverse
- Full Color Mechanical Symbols
  - Respects the colors of STEP model mapper
- Projection Settings added Orthographic projection
- Closest Distance – measure distance between two objects
- Handling Negative Space
- Selection Mode – select a window in 2D to show in 3D





Улучшения в PCB High Speed Option

- Reflection and Return path Visions (QIR7)
- L-Comp enhancement (QIR7)
- Via Structure enhancement (QIR7)

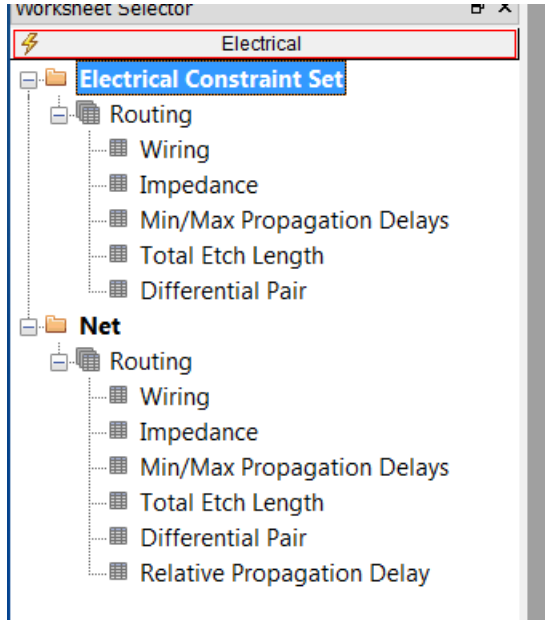


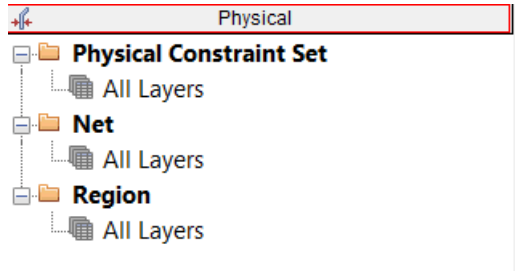
L-Comp Inductance Generator
Introduced in QIR4

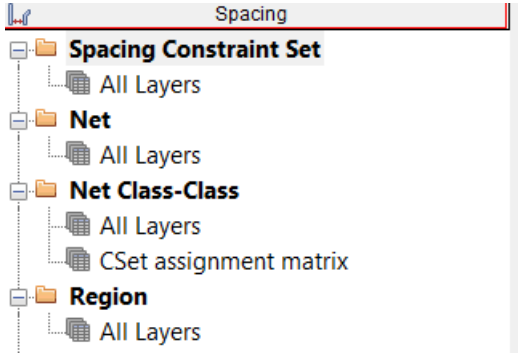
Добавление Constraint Manager в Capture 17.2 QIR7

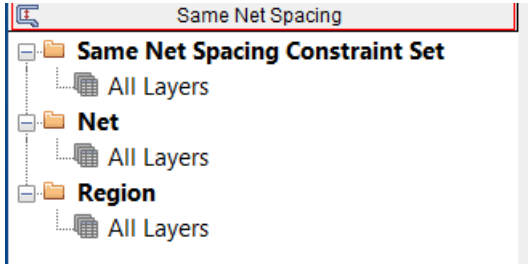
- Why Constraint Manger in Capture?
  - Capture users have been asking for constraint support for a long time
    - Familiar spreadsheet based structure
  - Customers are doing designs with DDR and other advanced interfaces
    - Require advanced constraints
  - Excellent Maintenance Upgrade opportunity for CCPs

- Electrical, Physical, Mechanical, and Manufacturing Rules
  - Wiring, Impedance, Propagation, Differential Pairs
  - Line, Pin, Pin Pairs, Via, Shape, Hole Spacing
  - Line, Neck Width, Differential Spacing



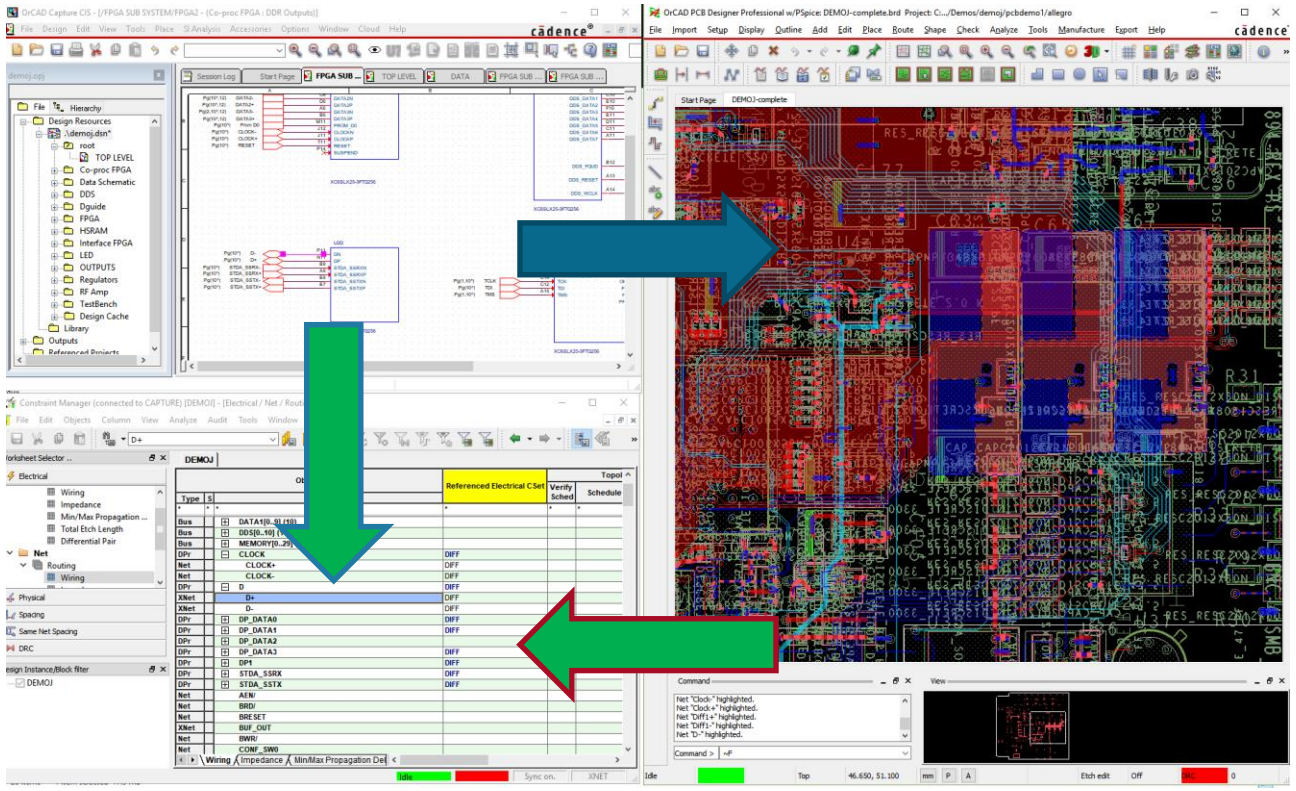






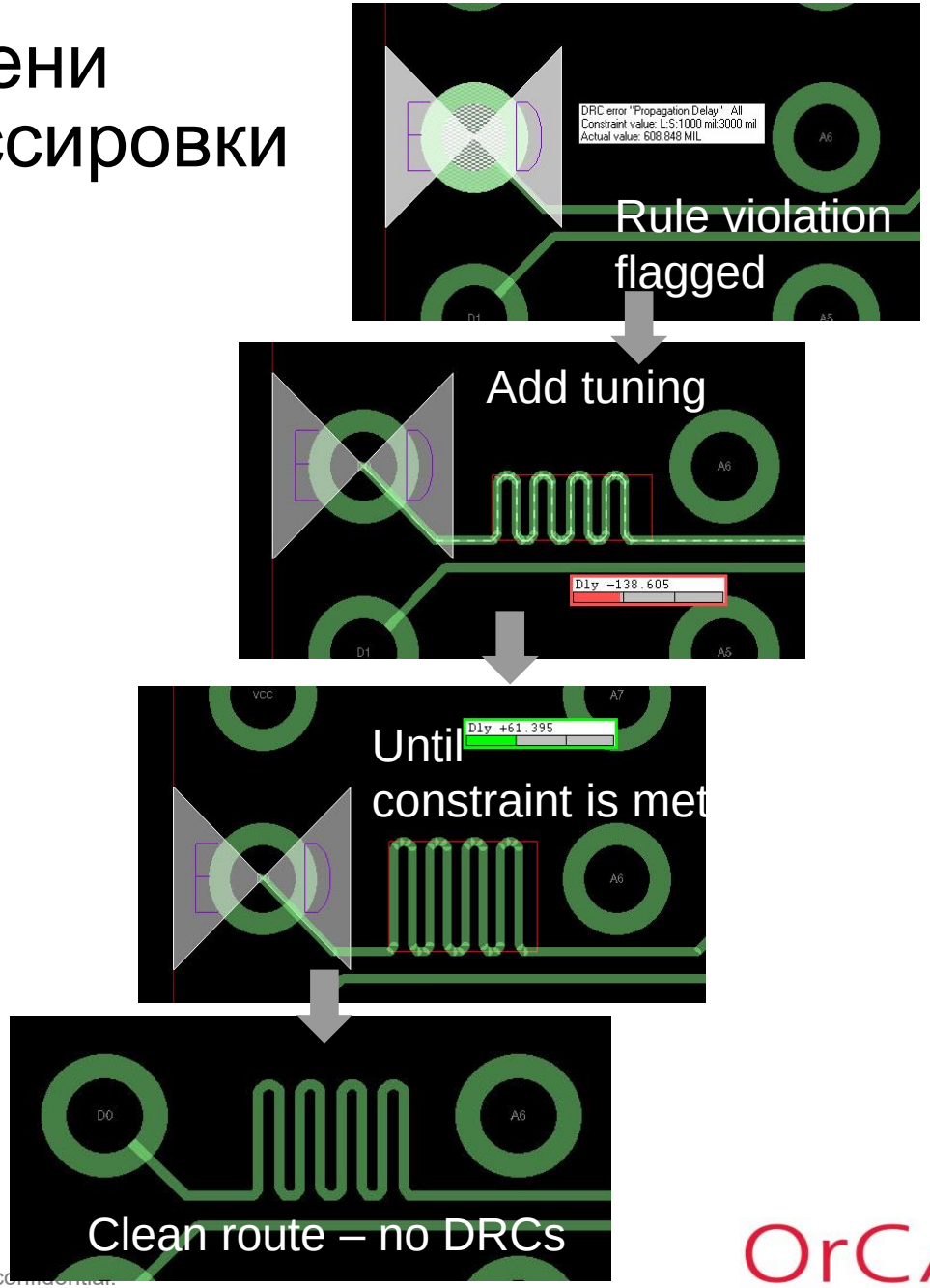
Полностью интегрированное решение

- Constraint driven flow enabled through ***ONE*** Constraint Manager
  - One GUI, one way to interact with CM whether the user is working with schematics or with SI or with layout; ***no translation of CONSTRAINTS***
  - Familiar spreadsheet based structure
  - Constraints part of design intent, travel with netlist to layout
  - Constraint Driven Floor planning, placement and interactive routing
  - Cross probe directly with design canvas
  - Search Constraint objects in Capture
  - Hierarchical rules support



Обратная связь в реальном времени Схемотехник задает правила трассировки

- Fix errors as they happen
  - Errors immediately displayed on screen
  - Real-time heads up display for length tuning
- Don’t compound problems
  - Prevent design decisions being made on incorrect assumptions



Capture – поддержка ограничений Constraint Manager

- Functionality of Capture CM aligned with CM functionality in corresponding tier of PCB Editor
- Capture/CIS standalone licenses will support PCB Designer Standard CM functionality

Product	CM Functionality
Capture Capture CIS Allegro Design Entry Capture Allegro Design Authoring - Capture CIS	OrCAD PCB Editor Standard
OrCAD PCB Designer Standard	OrCAD PCB Editor Standard
OrCAD PCB Designer Professional	OrCAD PCB Editor Professional

Поддержка Constraint Sets

Aligned with Appropriate Tier of PCB Editor

Constraints	PCB Designer Standard	PCB Designer Professional
Electrical Constraint Set	✓	✓
Physical Constraint Set	✓	✓
Spacing Constraint Set	✓	✓
Same Net Spacing	✓	✓
Constraints		
Differential pair	✓	✓
Xnet Visibility	✓	✓
Xnet Creation/Deletion		✓
Relative propagation delays		✓
Wiring		✓
Impedances		✓
Min/Max Propagation delays		✓
Total Etch length		✓

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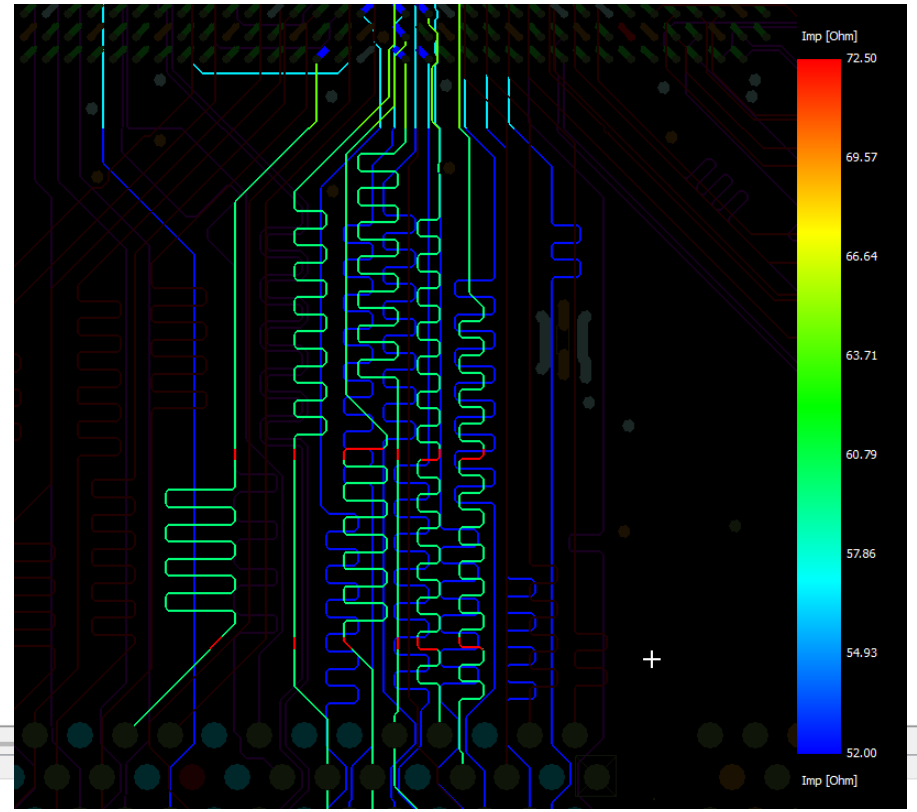
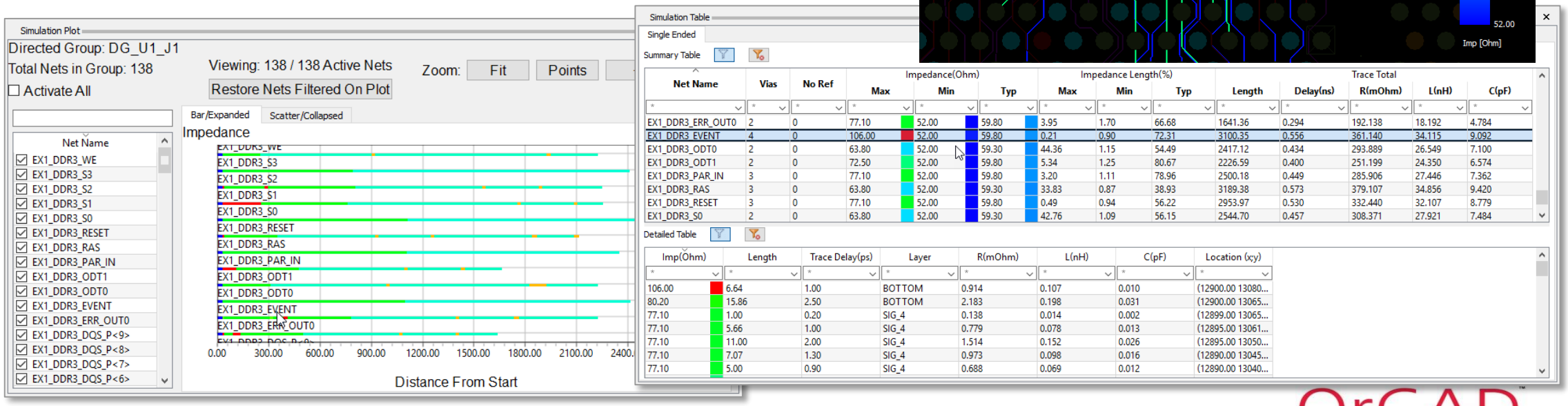
Улучшения QIR7– PCB Editor

Скрининг импеданса по всей плате

- Global view of results more accessible
  - Graphics
  - Tables
  - Plots
- Look for outliers





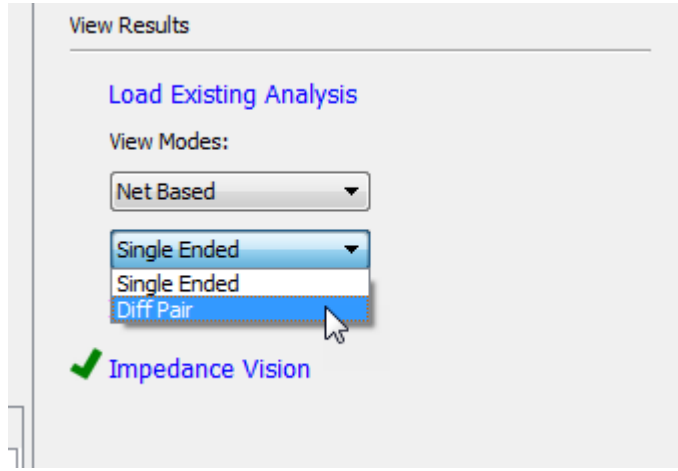
Net Name	Vias	No Ref	Impedance(Ohm) Max	Min	Typ	Impedance Length(%) Max	Min	Typ	Trace Total Length	Delay(ns)	R(mOhm)	L(nH)	C(pF)
EX1_DDR3_ERR_OUT0	2	0	77.10	52.00	59.80	3.95	1.70	66.68	1641.36	0.294	192.138	18.192	4.784
EX1_DDR3_EVENT	4	0	106.00	52.00	59.80	0.21	0.90	72.31	3100.35	0.556	361.140	34.115	9.092
EX1_DDR3_ODT0	2	0	63.80	52.00	59.30	44.36	1.15	54.49	2417.12	0.434	293.889	26.549	7.100
EX1_DDR3_ODT1	2	0	72.50	52.00	59.80	5.34	1.25	80.67	2226.59	0.400	251.199	24.350	6.574
EX1_DDR3_PAR_IN	3	0	77.10	52.00	59.80	3.20	1.11	78.96	2500.18	0.449	285.906	27.446	7.362
EX1_DDR3_RAS	3	0	63.80	52.00	59.30	33.83	0.87	38.93	3189.38	0.573	379.107	34.856	9.420
EX1_DDR3_RESET	3	0	77.10	52.00	59.80	0.49	0.94	56.22	2953.97	0.530	332.440	32.107	8.779
EX1_DDR3_S0	2	0	63.80	52.00	59.30	42.76	1.09	56.15	2544.70	0.457	308.371	27.921	7.484

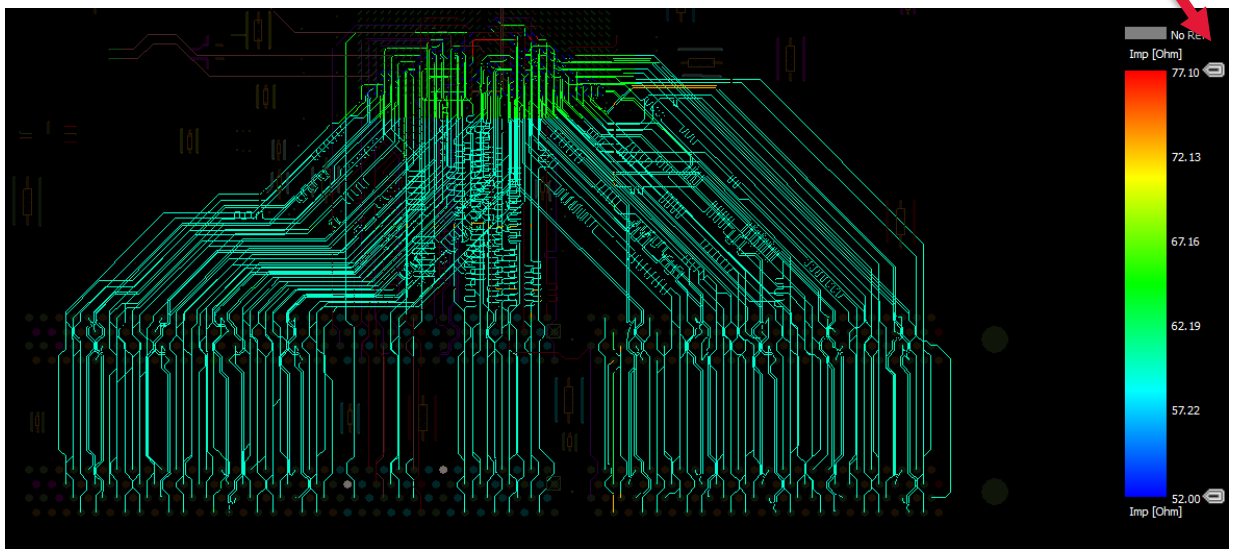
Imp(Ohm)	Length	Trace Delay(ps)	Layer	R(mOhm)	L(nH)	C(pF)	Location (x;y)
106.00	6.64	1.00	BOTTOM	0.914	0.107	0.010	(12900.00 13080...
80.20	15.86	2.50	BOTTOM	2.183	0.198	0.031	(12900.00 13065...
77.10	1.00	0.20	SIG_4	0.138	0.014	0.002	(12899.00 13065...
77.10	5.66	1.00	SIG_4	0.779	0.078	0.013	(12895.00 13061...
77.10	11.00	2.00	SIG_4	1.514	0.152	0.026	(12895.00 13050...
77.10	7.07	1.30	SIG_4	0.973	0.098	0.016	(12890.00 13045...
77.10	5.00	0.90	SIG_4	0.688	0.069	0.012	(12890.00 13040...

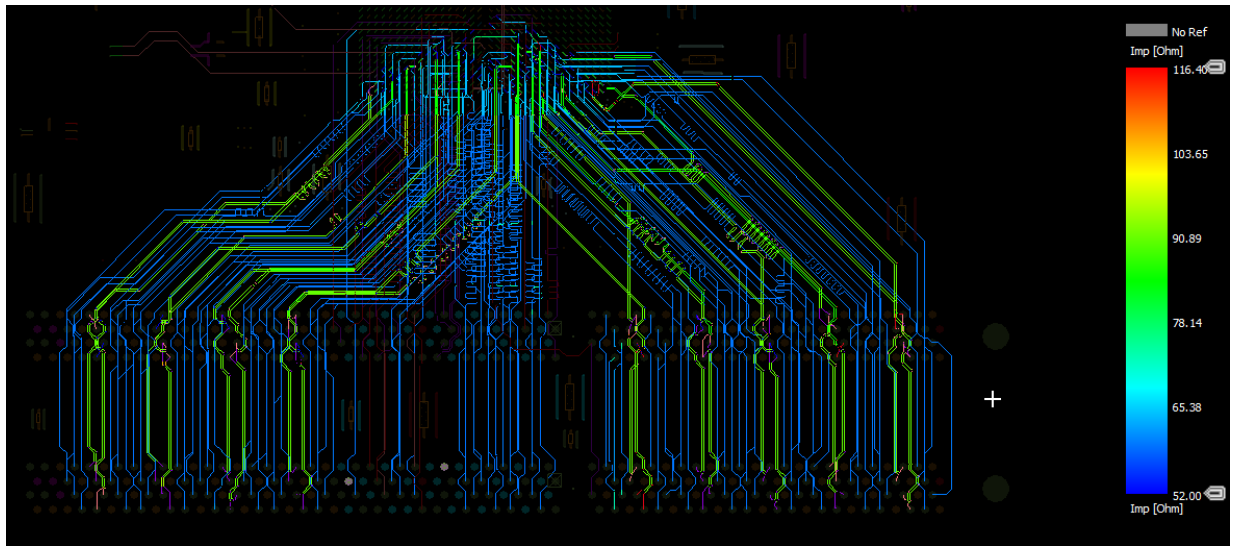
OrCAD CADENCE PCB SOLUTIONS

Анализ импеданса вдоль трассы, визуализация проблем

- Toggle between Single Ended and Diff Pair
  - Adds Diff Pair tab to table and toggles Diff Pairs views in Impedance Vision
  - Visions offer easy visual scan of outliers
  - Sliders on scale allow for filtering of view

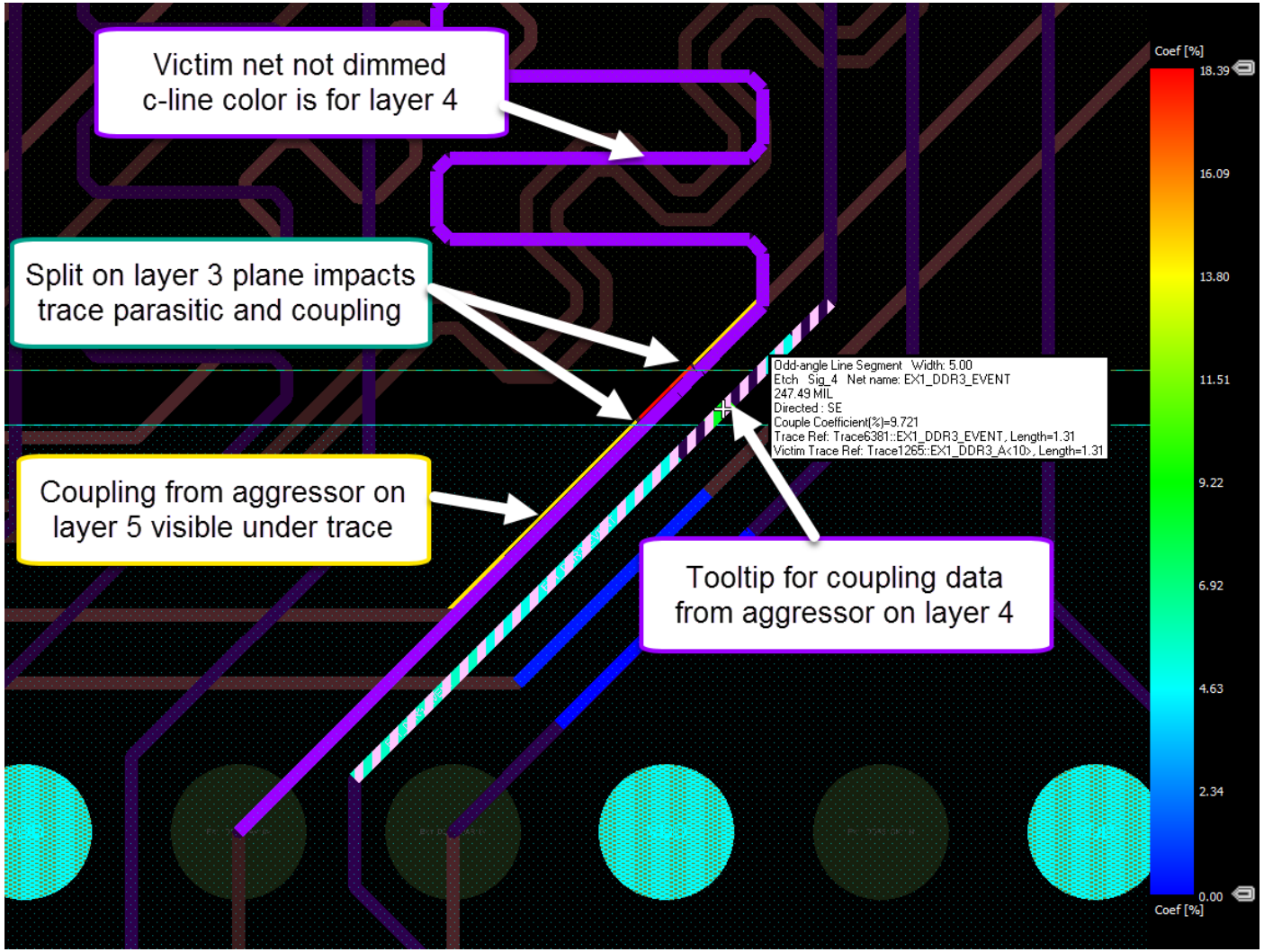






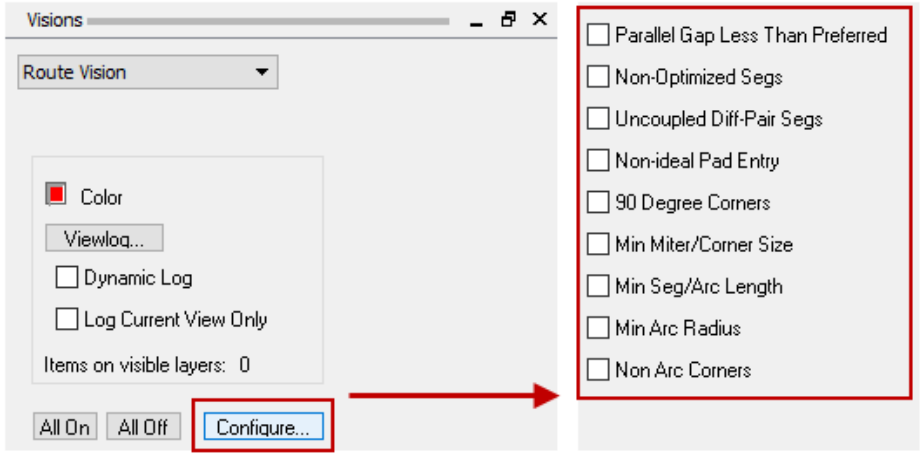
Анализ перекрестных помех, визуализация проблем

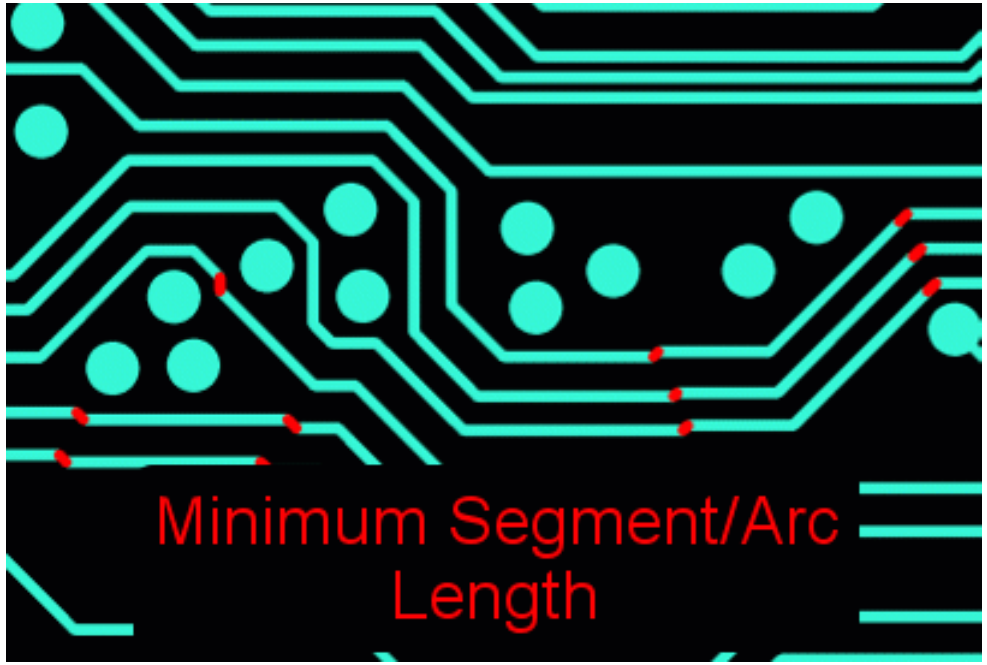
- No SI models required
- Quickly identify nets that are coupled
- Visions provide an easy way to detect issues and make decisions on what, how to fix



Анализ качества трассировки, визуализация проблем

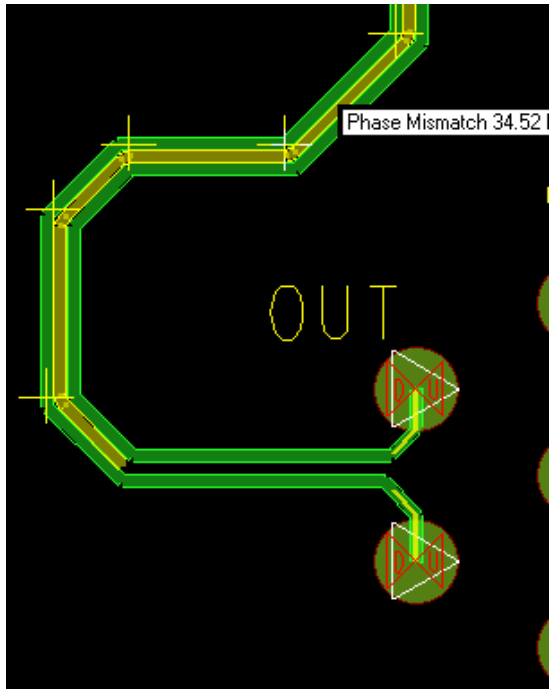
- Route Vision provides 9 users checks for improving route quality
- Customers want to improve design quality by identifying and optimizing various routing configurations
- Optimization issues can otherwise go unnoticed, and may or may not be caught by post-layout software, like cam systems

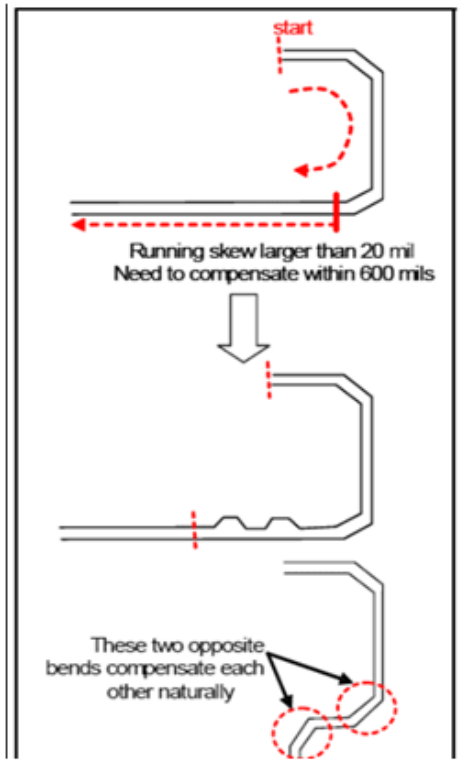




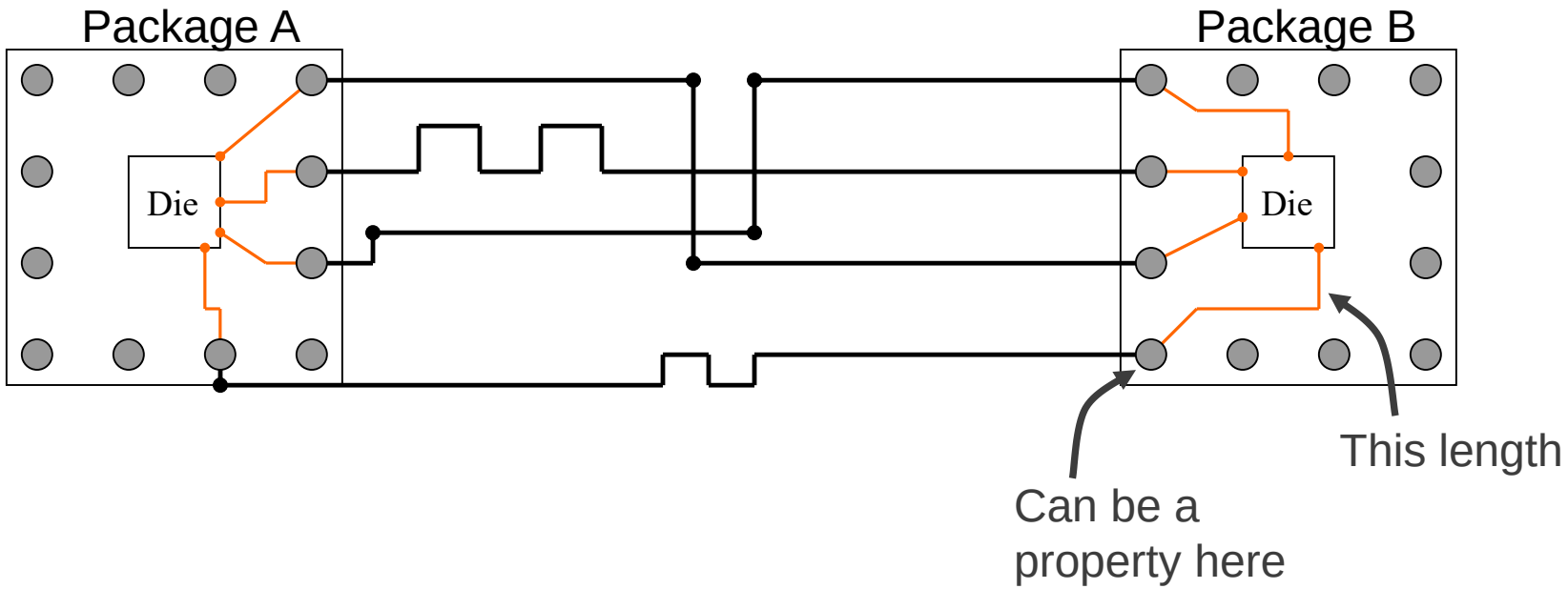
Динамический контроль фазы Dynamic Diff Pair Phase Control

- Phase matching of Diff Pairs required at trace bend points across the driver-receiver path
- Running skew rules require compensation within specified distance
  - Typical 600 mils
- Designers can add phase bumps or add zig-zags to meet the phase rule within the max length limit





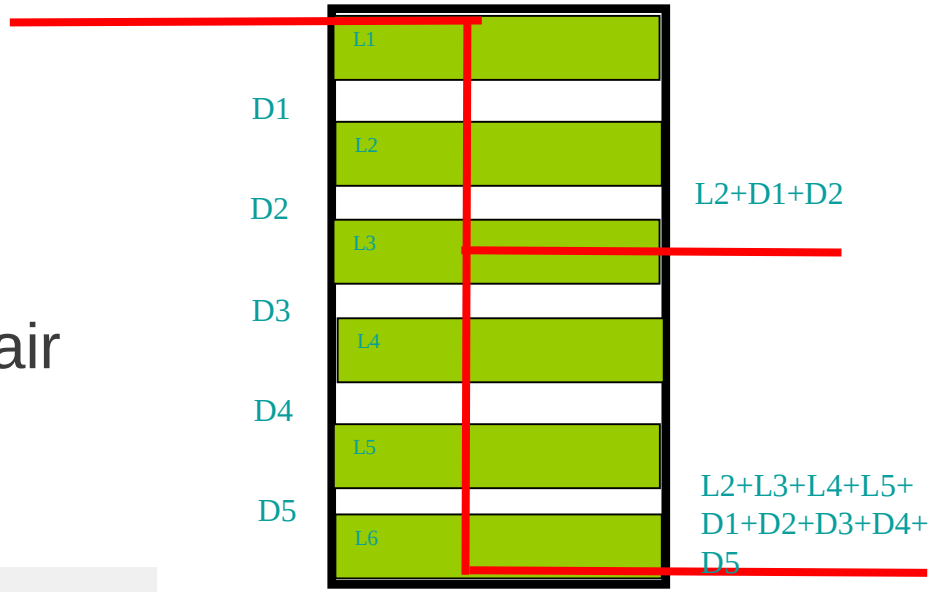
Учет задержки в микросхеме Pin Delay Property

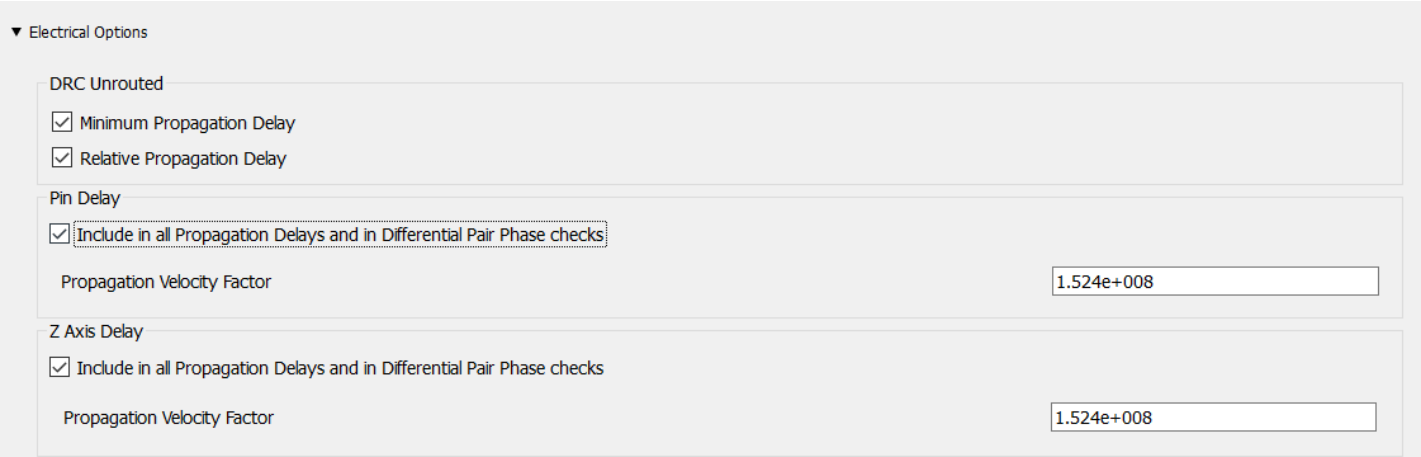


- Pin Delay property to represent extra delay
  - Length only
  - Can represent internal Package Delay for Die pad to Die pad constraints
  - Can represent external delay on daughter card for connector pin
  - Can be automatically extracted from APD package designs
  - Multiple input options

Учет задержки в отверстии Z-Axis Delay

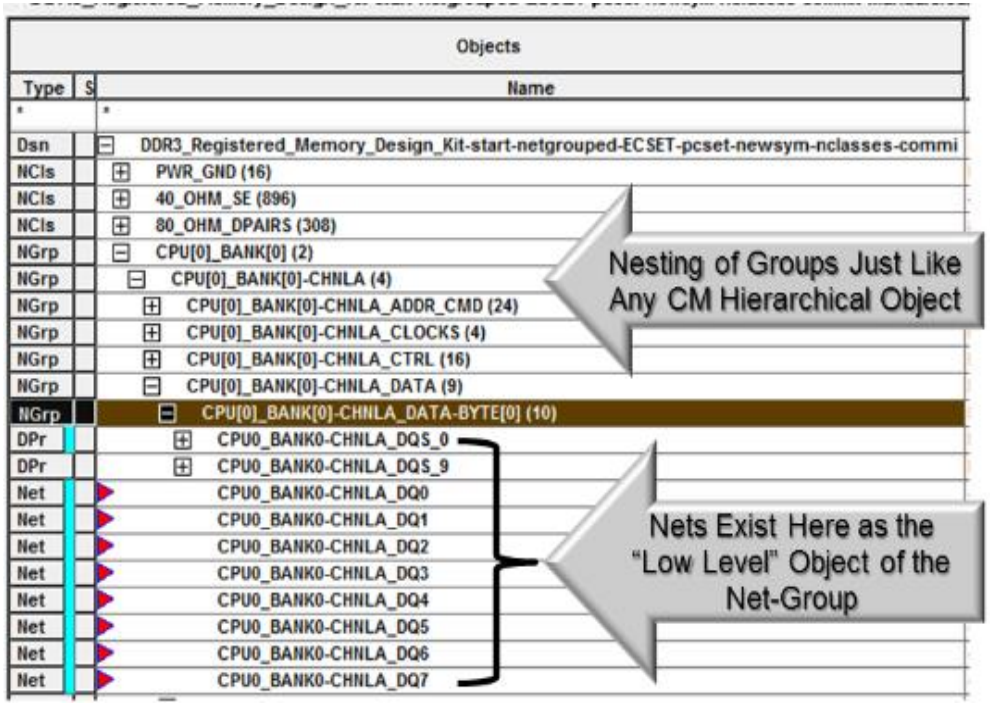
- Signal length down the barrel of a via or pin hole used to calculate timing path
- Works in conjunction with the Min/Max Propagation, Relative Propagation or Diff Pair Phase Control electrical rules

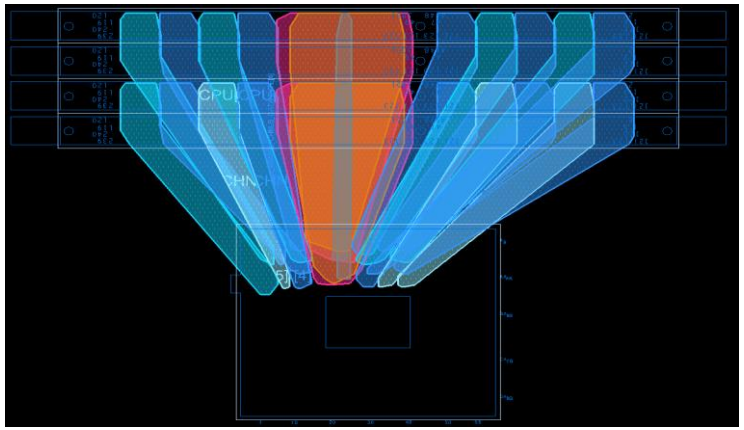




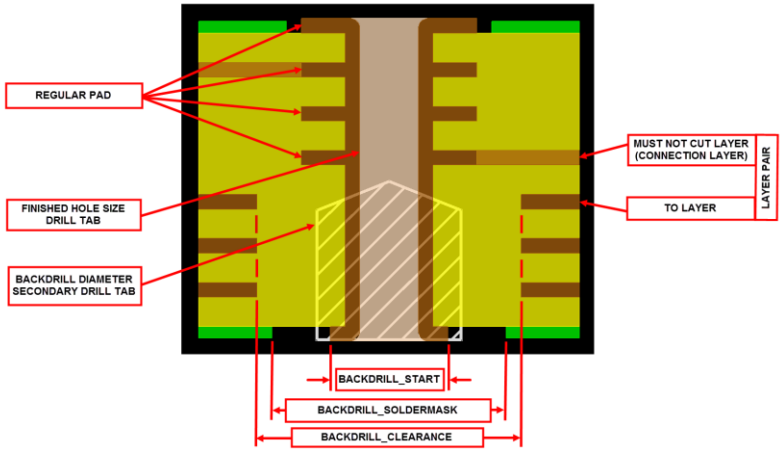
Вложенные Net Groups

- DDR memory system the signals can be divided into 4 groups - **ADDR/CMD**, **CTRL**, **CLOCKS** and **DATA**
- The largest group - **DATA** - can be further broken down into sub-groups called Byte-Lanes
- These Byte-Lanes lend themselves to be Net-Groups of their own while still remaining part of the bigger group called - **DATA**.

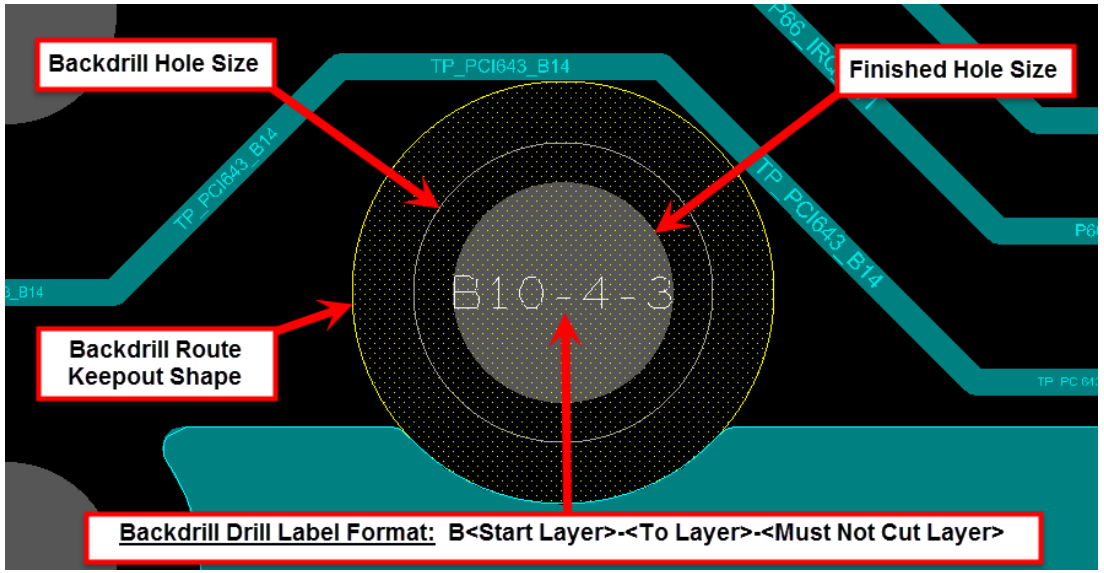




Продвинутые правила обратной сверловки Backdrill Rules



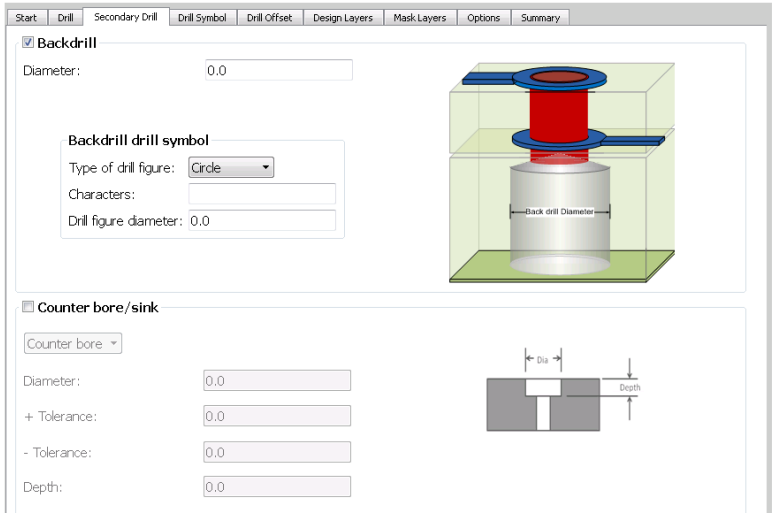
- Finished hole size, backdrill size
- Start layer and must not cut layer
- Backdrill clearance anti-pad size

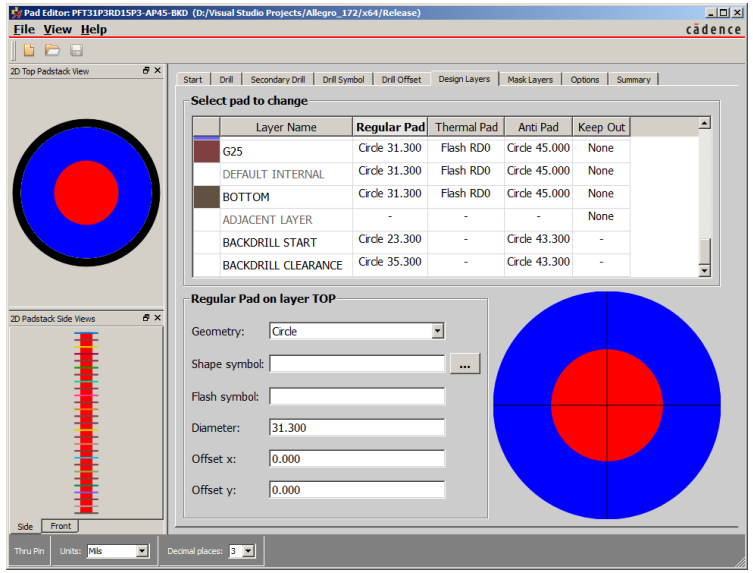


Backdrill locations clearly identified with special drill labels and hollow circle showing the backdrill diameter

Backdrill – модель работы на основе библиотеки

- Pad definition now supports:
  - Backdrill tool diameter
  - Figure and characters for legend
  - Clearance pad
  - Start layer pad/mask





- Backdrill analysis replaces regular pads with backdrill defined pads/clearances on backdrill path