cadence®

Cadence PCB Design Solutions

Industry leading PCB design solutions

Unlike other PCB design solutions, Cadence® OrCAD® and Allegro® PCB design suites can grow with future design needs and technology challenges. They provide a feature-rich, fully scalable solution that can be expanded and upgraded as the level of design sophistication grows.

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Schematic Capture & Data Management			
OrCAD Capture Schematic Entry	•	•	•
OrCAD Capture Market place for Apps, Models, Symbols and more	•	•	•
Graphical, flat and hierarchical page editor and Picture block hierarchy	•	•	•
Net Groups - Complex bus definition	•	•	•
Intelligent PDF creation	• (updated in 17.2)	• (updated in 17.2)	• (updated in 17.2)
AutoWire	•	•	•
44,000 Schematic symbols	•	•	•
3D Footprint Viewer	•	•	•
Color Components / nets	•	•	•
Tcl TK scripting support	•	•	•
Online design rule check including custom DRC capability and Waive DRC	•	•	•
Forward and back-annotation of properties / pin-and-gate swaps	•	•	•
Schematic Part and Library editor	•	•	•
Automated data extraction and symbol creation from PDF datasheet	OrCAD Library Builder	OrCAD Library Builder	OrCAD Library Builder
Cross-probing and cross-placing	•	•	•
FPGA design-in / pin import & export	•	•	•
Multiple PCB netlist interfaces	•	•	•
SI Topology creation	•	•	•
Property editor for pins, components, nets	•	•	•

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Digi-Key (PartLink App) Component Parametric data directly from web	•	•	•
Automated Graphical Design Compare	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Export ISCF (Intel schematic connectivity format)	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Import / Export XML	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Altium, PADS, Eagle CAD Importer (schematic and PCB)	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Allegro Design Authoring Schematic Entry			•
Component Information System	CIS option	CIS option	•
New part introduction capability	CIS option	CIS option	•
Interface to relational database and management systems	CIS option	CIS option	•
Database query for part selection and parametric properties	CIS option	CIS option	•
Manage multiple BOM variants	CIS option	CIS option	•
CIS Database Management Interface (access control and more)	OrCAD CIP	OrCAD CIP	CIP
Part search and download Digi-Key, FARNELL, FUTURE, MOUSER, ARROW, RS	OrCAD CIP (updated in 17.2)	OrCAD CIP (updated in 17.2)	CIP (updated in 17.2)
Assign user roles, page responsibilities, and track progress	OrCAD EDM	OrCAD EDM	Allegro Team Design Option
Lock projects / pages for editing or view only	OrCAD EDM	OrCAD EDM	Allegro Team Design Option
Manage and track schematic page and project revisions	OrCAD EDM	OrCAD EDM	Allegro Team Design Option
Symbol level library sharing and revision handling	OrCAD EDM	OrCAD EDM	Allegro Team Design Option
Analog Simulation			
33,000 Part Pspice Model Starter Library	PSpice AD	PSpice AD	PSpice AD
Multi-core engine support	PSpice AD	PSpice AD	PSpice AD
DC sweep, AC sweep, & transient analysis	PSpice AD	PSpice AD	PSpice AD
Auto-Convergence Engine	PSpice AD	PSpice AD	PSpice AD
Analog behavioral modelling	PSpice AD	PSpice AD	PSpice AD
Stimulus editor	PSpice AD	PSpice AD	PSpice AD
Model Editor for device characterization	PSpice AD	PSpice AD	PSpice AD
Magnetics Part Editor	PSpice AD	PSpice AD	PSpice AD
Interactive waveform viewer & analyzer	PSpice AD	PSpice AD	PSpice AD
IBIS / DML model support	PSpice AD	PSpice AD	PSpice AD
PSpice Modeling apps including: Sources, Transformers, TVS, VCO and Switches	PSpice AD	PSpice AD	PSpice AD
Open API for custom analysis and post-processing	PSpice AD	PSpice AD	PSpice AD
Sensitivity: Identifies critical circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Optimizer: Optimizes key circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
Monte Carlo: Analyzes statistical circuit behavior and yield	Advanced Analysis	Advanced Analysis	Advanced Analysis
Smoke: Detects component stress	Advanced Analysis	Advanced Analysis	Advanced Analysis
Parametric Plotter: Examine solution through nested sweeps	Advanced Analysis	Advanced Analysis	Advanced Analysis
SystemC / C++, Verilog A, Verilog AMS Modeling and Analysis	Advanced Analysis (updated in 17.2)	Advanced Analysis (updated in 17.2)	Advanced Analysis (updated in 17.2)
Signal Integrity			
Pre Route Signal Integrity Analysis	•	•	•
Graphical topology definition and exploration	•	•	•
Interactive waveform viewer	•	•	•
Macro modelling support (DML)	•	•	•
IBIS 5.0 support	•	•	•
IBIS ICM model support	•	•	•
Spectre-to-DML	•	•	•
HSPICE-to-IBIS	•	•	•
Lossy transmission lines	•	•	•
Coupled (3 net) simulation	•	•	•
Differential pair exploration and simulation	•	•	•
Post Route Signal Integrity Analysis		•	•
Net extraction from PCB Editor		•	•
Differential Pair Extraction from PCB Editor		•	•
Coupled (>3 net) exploration and simulation		•	•
Full SI Analysis and Verification	OrCAD PCB SI	OrCAD PCB SI	OrCAD PCB SI
Electrical Rule Check: Impedance discontinuities	OrCAD Sigrity ERC	OrCAD Sigrity ERC	OrCAD Sigrity ERC
Electrical Rule Check: Coupling areas with other signals	OrCAD Sigrity ERC	OrCAD Sigrity ERC	OrCAD Sigrity ERC
Electrical Rule Check: Phase differences of diff pairs	OrCAD Sigrity ERC	OrCAD Sigrity ERC	OrCAD Sigrity ERC
Electrical Rule Check: Number of vias	OrCAD Sigrity ERC	OrCAD Sigrity ERC	OrCAD Sigrity ERC
PCB Layout and Interactive Routing			
Unlimited Database	•	•	•
Netlist / Crossplace / Crossprobe	•	•	•
Padstack & Footprint Editor	• (updated in 17.2)	• (updated in 17.2)	• (updated in 17.2)
Cross Section Editor	• (updated in 17.2)	• (updated in 17.2)	• (updated in 17.2)
3D Visualization / Flipboard	•	•	•
Customizable, Automated Drill Legend / NC Output	•	•	•
Via-in-Pad Rules, Blind / Buried Via Support	•	•	•
Autoplacement / Quickplace / Floorplanner	•	•	•
Dynamic Shapes with Real-Time Plowing & Healing	•	•	•

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2D Drafting and Dimensioning	•	•	•
Multiple UNDO / REDO	•	•	•
Gerber 274X, 274D Artwork Output Generation	•	•	•
IPC-2581 Export	•	•	•
HTML-based Reports	•	•	•
DFM DRCs (exposed copper, slivers, pastemask, etc.)	•	•	•
Automatic Silkscreen Generation	•	•	•
Split Plane Support	•	•	•
SKILL (programming language) Runtime, Macro, & Scripting Support	•	•	•
Variant Assembly Drawing / Bill-of Material Creation	•	•	•
PCB Imports: PADS, P-CAD, Altium, Eagle (Schematic and PCB)	• (updated in 17.2)	• (updated in 17.2)	• (updated in 17.2)
Mechanical CAD Interface: IDF 3.0, IDX, DXF, STEP	•	•	•
Native 3D Viewer (STEP & Simple Extrusions)	•	•	•
MCAD/ECAD Incremental design data exchange (EDMD)	•	•	•
Snap Functions (precise drafting of lines /shapes)	•	•	•
SameNet Clearance DRC Support	•	•	•
Stacked Via Edit, Move	•	•	•
Single-sided Design Jumper Support	•	•	•
Physical and Spacing rules	• (NEW in 17.2)	•	•
Class-to-Class Net Spacing rules	• (NEW in 17.2)	•	•
SameNet Rules	• (NEW in 17.2)	•	•
Properties & DRC	•	•	•
Floorplanning, Autoplace	•	•	•
Place by room / by schematic page	•	•	•
Dynamic Shapes	•	•	•
Scribble Route	•	•	•
Snake Routing (Hex Pitch BGA)	•	•	•
Multi-line routing	•	•	•
Fan-out generators	•	•	•
Dynamic pad suppression / unused pad removal	•	•	•
Soldermask, Solderpaste checks	•	•	•
Component Height Checks	•	•	•
Multi-Core Support for Shapes & DRCs	•	•	•
DFT: Manual Test prep (test point generation & reuse)	•	•	•

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Pad Entry / Exit Rules	•	•	•
Multi-Cross Section Support (Flex)	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Zone Placement (Flex)	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Curve Routing (Flex)	•	•	•
Blind / Buried Microvia Stacking, Split, & Merge support	• (NEW in 17.2)	•	•
Dynamic Cross Hatch and Solid Planes (Flex)	• (NEW in 17.2)	• (NEW in 17.2)	• (NEW in 17.2)
Differential Pair Rules	• (NEW in 17.2)	•	•
Differential pair static phase control rules	• (NEW in 17.2)	•	•
IPC 7351 Complaint Footprint Creation	OrCAD Library Builder	OrCAD Library Builder	OrCAD Library Builder
Automated 3D STEP Model Creation and Alignment	OrCAD Library Builder	OrCAD Library Builder	OrCAD Library Builder
Hug Contour Routing (Flex)		•	•
Segment over void detection		• (NEW in 17.2)	•
Layer set rules		• (NEW in 17.2)	•
Extended Net creation		• (NEW in 17.2)	•
Matched group rules		• (NEW in 17.2)	•
Dynamic shape based filleting, line fattening and trace filleting		• (NEW in 17.2)	•
Dynamic Zone Placement (Flex)		• (NEW in 17.2)	• (NEW in 17.2)
Inter-Layer DRC Checks (Flex)		• (NEW in 17.2)	• (NEW in 17.2)
Zone Table Chart (Flex)		• (NEW in 17.2)	• (NEW in 17.2)
DFT: Auto Test Prep		•	•
Interactive Delay Tuning		•	•
Shape based curve fillet support, tapered traces		•	•
Placement Replication		•	•
Design For Fabrication (DFF) Checks		•	•
Region based rules (Rigid-Flex; BGA regions)		•	•
Constraint Regions		•	•
Min/Max length constraints		•	•
Constraint adherence feedback (red, green, yellow)		•	•
Dynamic heads-up display for critical rules		•	•
Single-ended Impedance Constraints		•	•
Group route via pattern		•	•
Propagation delay rules (Min/Max, Relative)		•	•

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T-Point rules (pin to T-Point) T-Point rules (pin to T-Point)		•	•
Via array / Shielding		•	•
Dynamic Differential Pair Phase Control rules			•
Dynamic DFA rules based interactive placement			•
Backdrilling			•
Enhanced Curved Routing			• (NEW in 17.2)
Electrical Constraint rule set (ECSets) / Topology Apply			• (NEW in 17.2)
Schematic based module reuse			•
Extended (X) net rules			•
Estimated Crosstalk rules			•
Max via count rules			•
Spread lines between anti-pads			•
Offset routing			•
Pin Pair rules			•
Mentor Boardstation Import			•
Dynamic Fillet Support			•
High-Speed rules based autorouting			•
Differential Pair Autorouting, Automatic net shielding			•
Design planning - Create hierarchical Bundles			•
Design planning - Create, Edit Flows			•
Design planning - Assign Flows to Layers			•
Design planning Assign Layers			•
Package Pin Delay (for die-2-die delay) rules			• (NEW in 17.2)
Z-Axis delay feedback			• (NEW in 17.2)
Advanced Constraints (formulas, relational)			• (NEW in 17.2)
Electrical rules (Reflection, Timing, Crosstalk)			• (NEW in 17.2)
Unused micro-via removal			• (NEW in 17.2)
Design Planning - Plan Spatial Feasibility analysis & feedback			Design Planning Option (PA3670)
Design Planning - Generate Topological Plan			Design Planning Option (PA3670)
Design Planning - Auto-interactive Breakout Technology (AiBT)			Design Planning Option (PA3670)
Design Planning - Convert Topological plan to traces (CLINES)			Design Planning Option (PA3670)
Design Planning - Auto-interactive adjust spacing			Design Planning Option (PA3670)
Backdrilling - Library Driven			PCB High Speed Option (PA3110)

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Auto Interactive Delay Tune (AiDT)			PCB High-Speed Option (PA3110)
Auto Interactive Phase Tune (AiPT)			PCB High-Speed Option (PA3110)
TimingVision advanced timing closure engine			PCB High-Speed Option (PA3110)
Fiber Weave Off-Angle Routing			PCB High-Speed Option (PA3110)
Differential Pair Return Path Vias			PCB High-Speed Option (PA3110)
Tabbed Routing (Intel)			PCB High-Speed Option (PA3110) (NEW in 17.2)
High Speed Differential Pair Via Structures (Sigrity Integration)			PCB High-Speed Option (PA3110) (NEW in 17.2)
Fabric Weave Routing			PCB High-Speed Option (PA3110) (NEW in 17.2)
Single Net and Diff Pair Return Path Via Templates			PCB High-Speed Option (PA3110) ((NEW in 17.2)
HDI Micro-via (spacing, stacking) rules			Miniaturization Option (PA3120)
HDI micro-via inset (via-in-pad) rules			Miniaturization Option (PA3120)
HDI micro-via stack editing			Miniaturization Option (PA3120)
Single Click multiple micro-via instantiation			Miniaturization Option (PA3120)
Manufacturing rule support for embedding components			Miniaturization Option (PA3120)
Embedded Packaged Components			Miniaturization Option (PA3120)
Support for Cavities on inner layers			Miniaturization Option (PA3120)
Concurrent Team Design - Layer by Layer partitioning			PCB Team Design Option (PA3410)
Concurrent Team Design - Functional block partitioning			PCB Team Design Option (PA3410)
Concurrent Team Design - Team design dashboard			PCB Team Design Option (PA3410)
Concurrent Team Design - Soft nets			PCB Team Design Option (PA3410)
Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner (PA8250)
Re-optimize pins on a FPGA (using FPGA rules)			FPGA System Planner (PA8250)
Parameterized RF etch elements			PCB Analog / RF Option (PA3420)
Asymmetrical Clearances			PCB Analog / RF Option (PA3420)
RF Etch elements editing			PCB Analog / RF Option (PA3420)

Feature	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Bidirectional interface with Agilent ADS			PCB Analog / RF Option (PA3420)
Import Agilent ADS schematics into DE HDL			PCB Analog / RF Option (PA3420)
Layout-driven RF design creation			PCB Analog / RF Option (PA3420)
Flexible Shape Editor			PCB Analog / RF Option (PA3420)
Via Array placement on traces, shapes			PCB Analog / RF Option (PA3420)
Create intelligent PDF output from Board Design			Design Publisher Option (PA1220)
Autorouting			
6 Signal Layers at a time (no board layer limit or pin limit)		•	•
Shape-based or Grid routing		•	•
SMD Fanout		•	•
Trace Width by Net and Net Classes		•	•
45-degree / Memory Pattern Routing		•	•
Interactive Routing with Shoving and Plowing		•	•
Interactive Floorplanning		•	•
Online Design Rule Checking		•	•
Flip, Rotate, Align, Push, and Move Components		•	•
Placement Density Analysis		•	•
High Speed rules based autorouting			•
Min/Max, matched length rules based autorouting			•
Pin-pair rules, Area rules based autorouting			•
Crosstalk controls, parallelism rules based autorouting			•
Differential Pair Autorouting, Automatic net shielding			•
High-speed rules-based autorouting			•
256 signal layer limit		OrCAD Router Auto / Interactive Option	PCB Routing Option
DFM rules-based autorouting			PCB Routing Option
Automatic trace spreading			PCB Routing Option
ATP generation			PCB Routing Option
Layer-specific rules-based autorouting			PCB Routing Option

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